Configuring the JUNOS Software to Support the Sparse DLCI Mode on Channelized STM1 or Channelized DS3 PICs

By default, original channelized DS3 and original channelized STM1-to-E1 (or T1) interfaces can support a maximum of 64 data-link connection identifiers (DLCIs) per channel—as many as 1792 DLCIs per DS3 interface or 4032 DLCIs per STM1 interface (0 through 63).

In sparse DLCI mode, the full DLCI range (1 through 1022) is supported. This allows you to use circuit cross-connect (CCC) and translation cross-connect (TCC) features by means of Frame Relay on T1 and E1 interfaces.

NOTE: Sparse DLCI mode requires a Channelized STM1 or Channelized DS3 PIC.

DLCI 0 is reserved for Local Management Interface (LMI) signaling.

Channelized T3 (CT3) intelligent queuing (IQ) and STM1 IQ interfaces support a maximum of 64 DLCIs, numbered 0 through 1022, and therefore do not require sparse mode.

The CT3 PIC must use field-programmable gate array (FPGA) hardware revision 17 to run sparse DLCI mode.

To configure the router to use sparse DLCI mode, include the sparse-dlcis statement at the [edit chassis fpc *slot-number* pic *pic-number*] hierarchy level:

```
[edit chassis fpc slot-number pic pic-number ]
sparse-dlcis;
```

Related Topics

- Configuring the JUNOS Software to Enable a SONET PIC to Operate in Channelized (Multiplexed) Mode
- Configuring the JUNOS Software to Support Channelized DS3-to-DS0 Naming for Channel Groups and Time Slots
- Configuring the JUNOS Software to Support Channel Groups and Time Slots for Channelized E1 PICs
- Configuring the JUNOS Software to Support Channelized STM1 Interface Virtual Tributary Mapping
- Configuring the JUNOS Software to Enable Larger Delay Buffers for T1, E1, and DS0 Interfaces Configured on Channelized IQ PICs

Published: 2010-04-26