Structure of Channelized IQ and Channelized IQE PICs

Figure 1 through Figure 13 show the structural organization of the channelized PICs, channelized IQ PICs, and channelized IQE PICs. Table 1 through Table 3 show the structure of channelized IQE PICs, channelized IQ PICs, and channelized PICs.

Figure 1: Channelized OC48/STM16 IQE PIC (in SONET Mode)

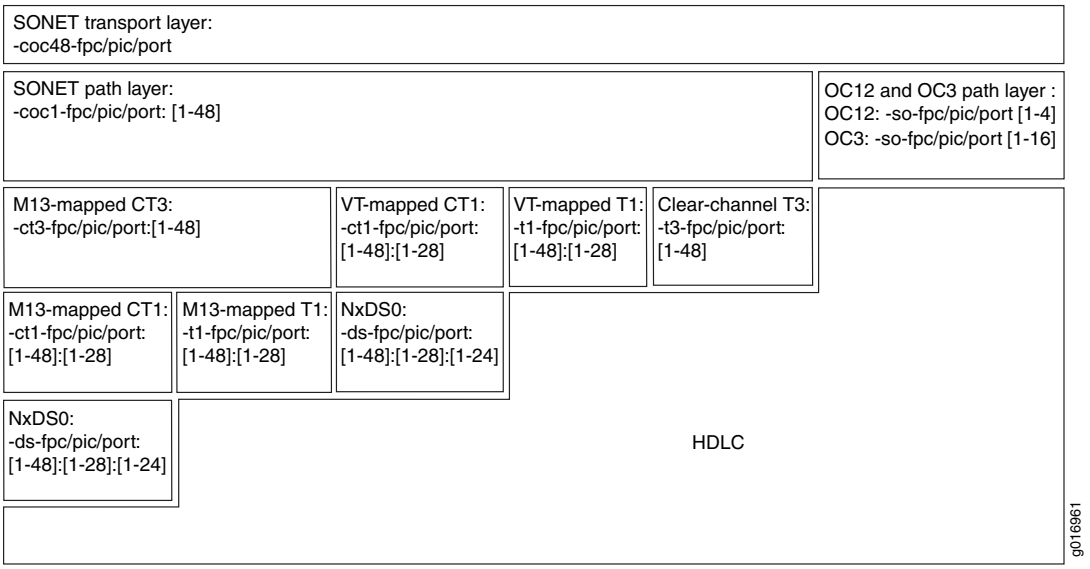

Figure 2: Channelized OC48/STM16 IQE PIC (in SDH Mode)

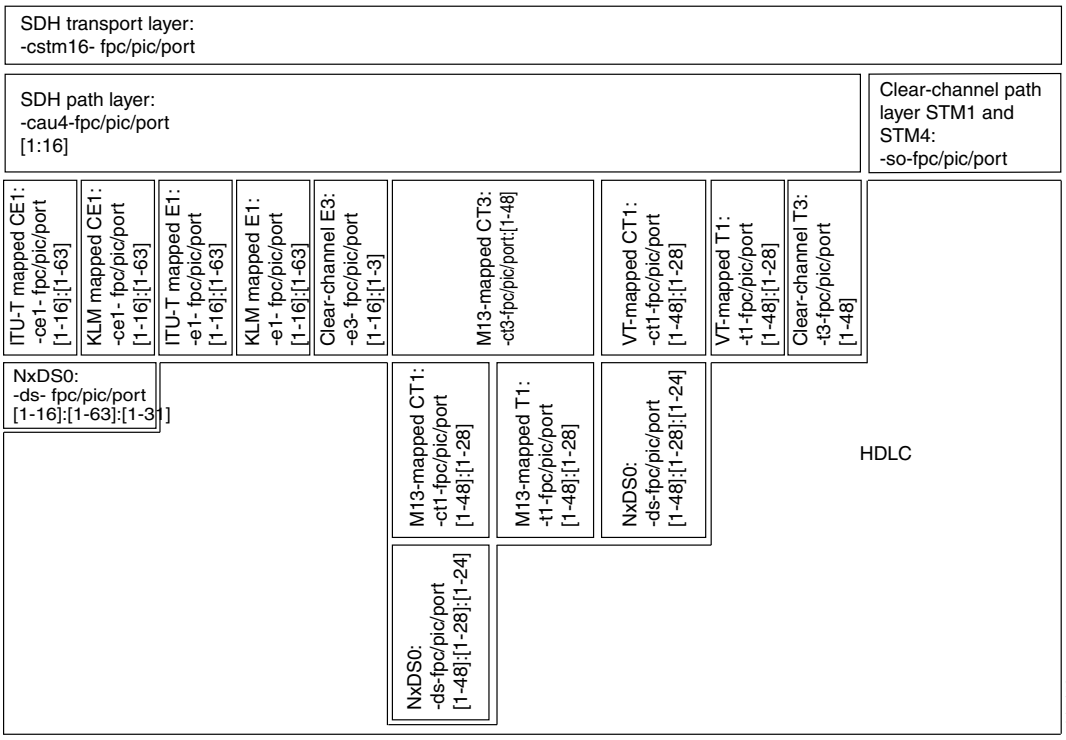

Figure 3: Channelized OC12 IQ PIC and Channelized OC12/STM4 IQE PIC (in SONET Mode)

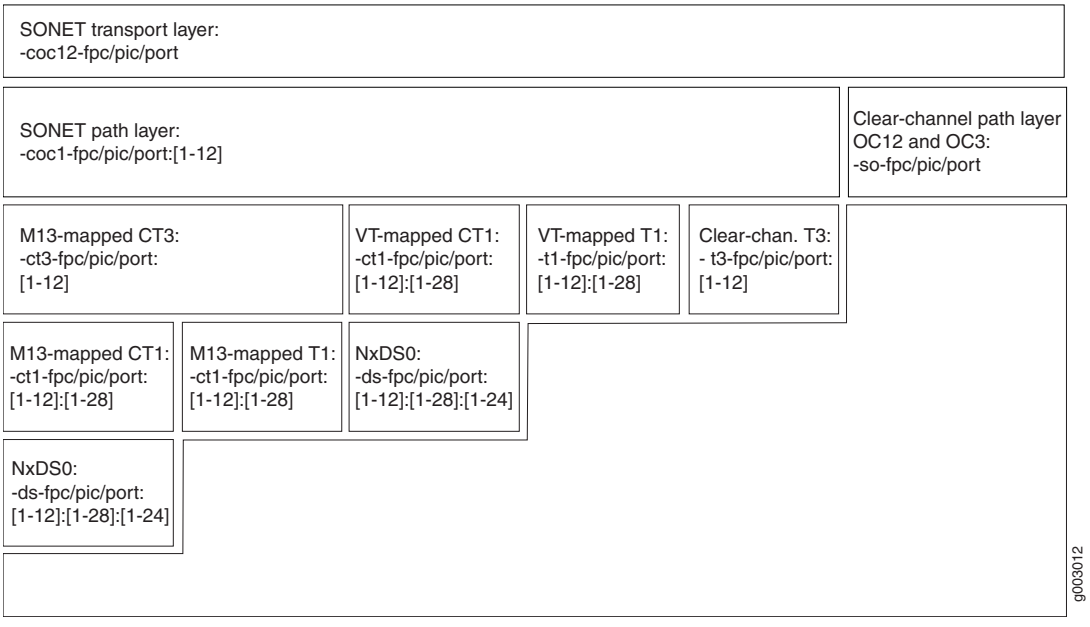

Figure 4: Channelized OC12/STM4 IQE PIC (in SDH Mode)

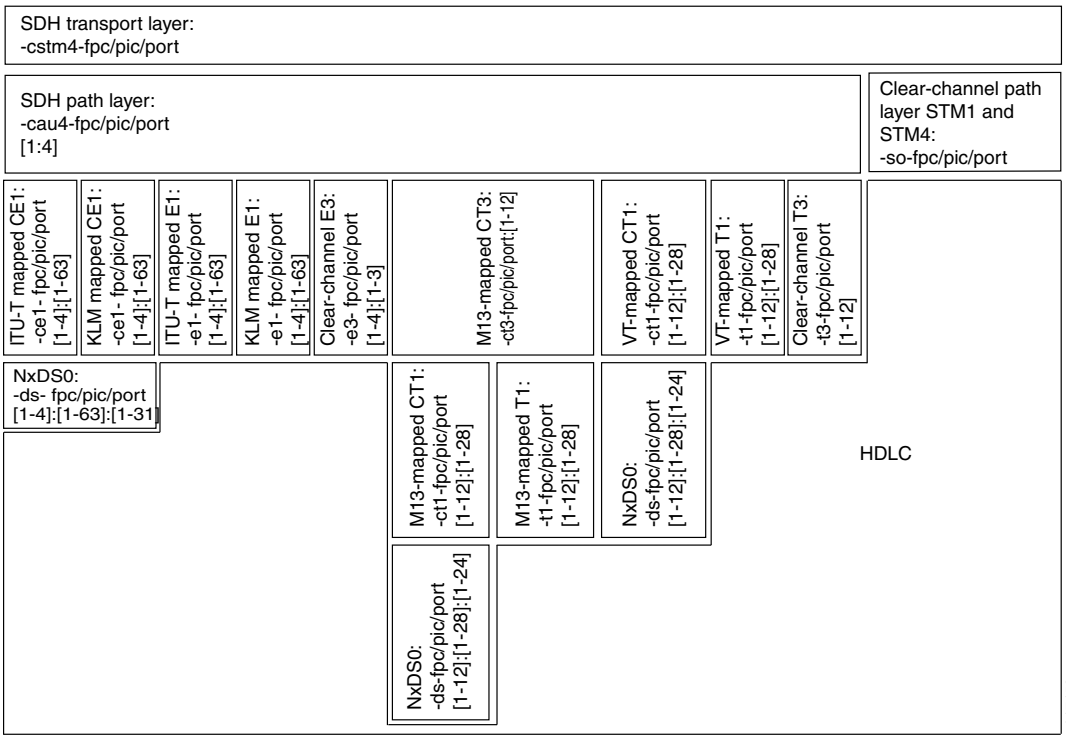

Figure 5: Channelized OC12/STM4 IQ PIC (in SDH Mode)

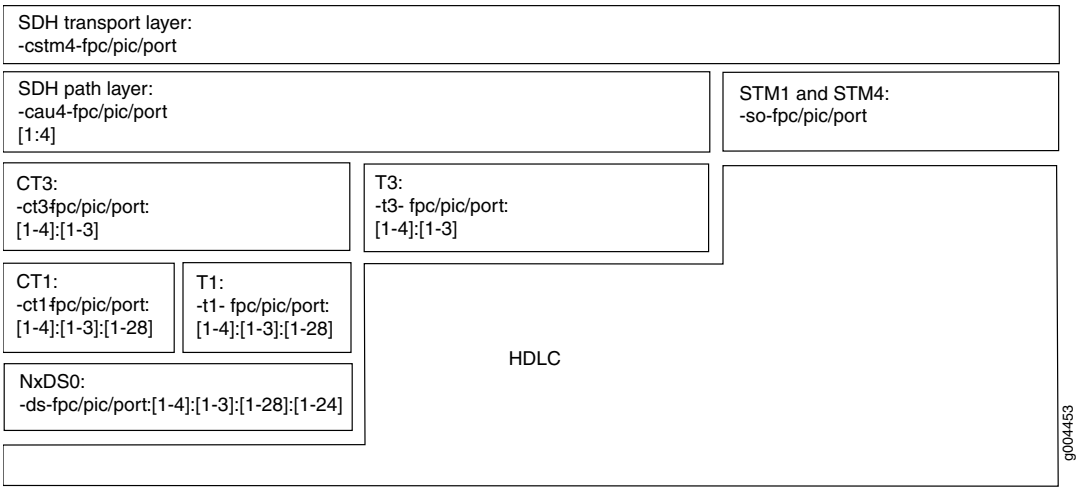

Figure 6: Channelized OC3 Ports (in SONET Mode) on Channelized OC3 IQ and Channelized OC3/STM1 IQE PICs

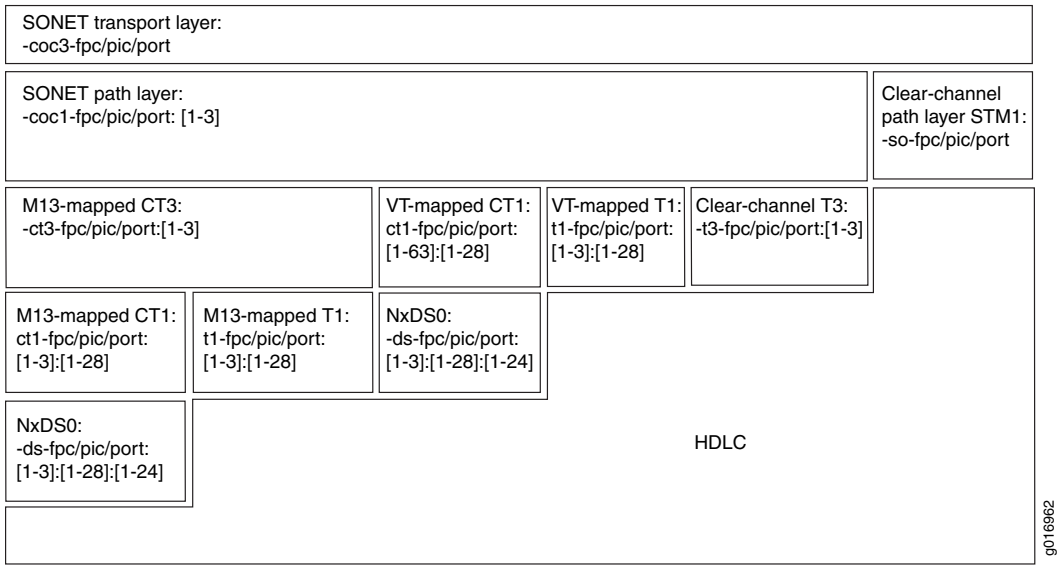

Figure 7: Channelized CSTM1 Ports (in SDH Mode) on Channelized OC3/STM1 IQE PIC

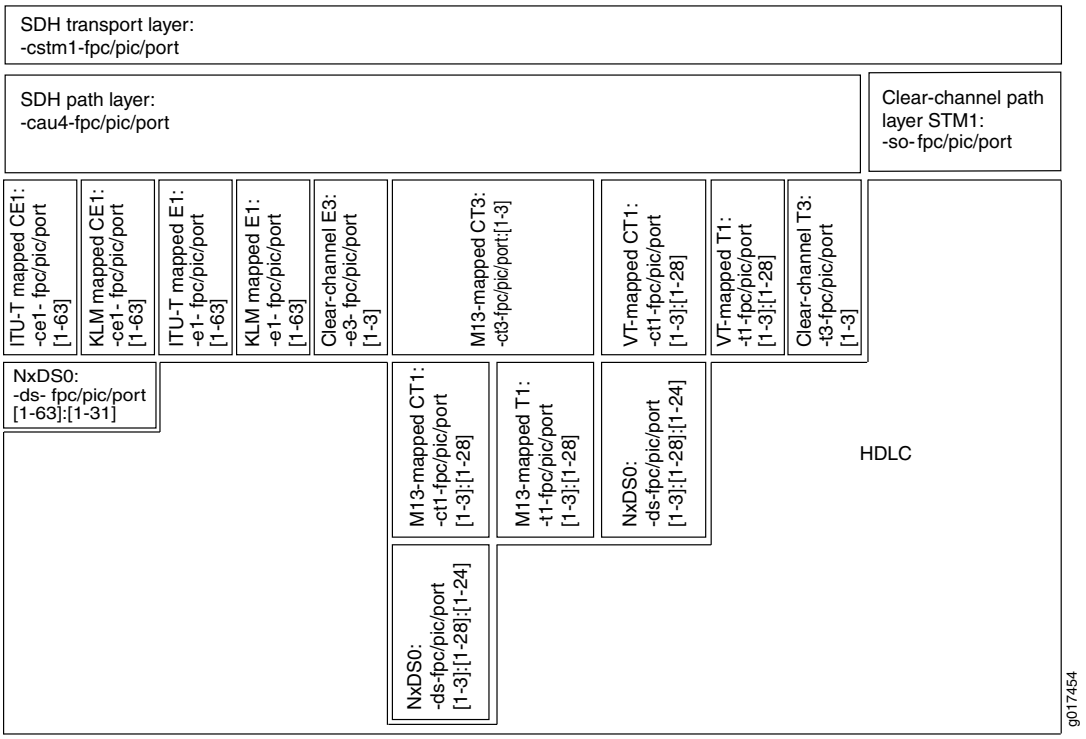

Figure 8: Channelized STM1 IQ PIC

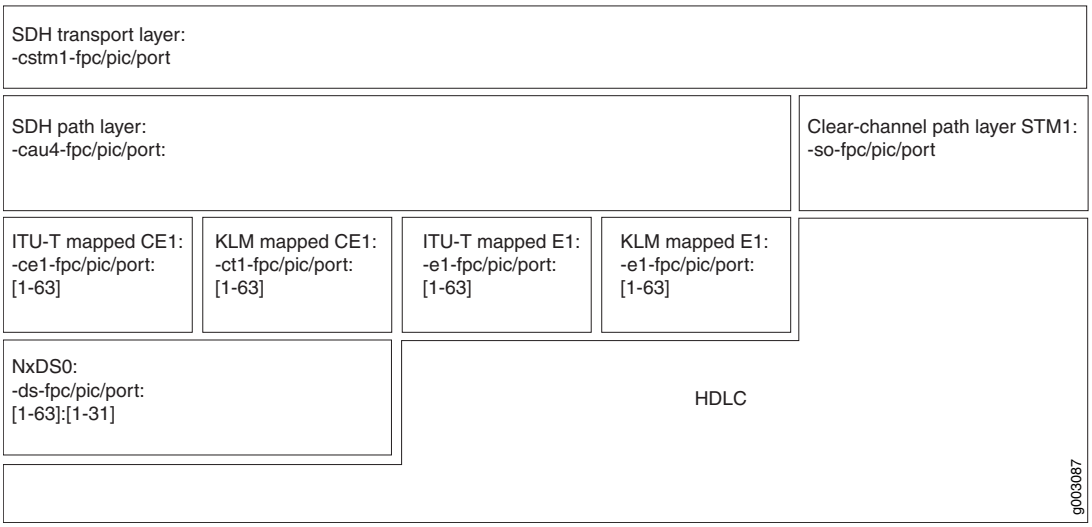

Figure 9: Channelized CDS3/E3 IQE PIC (in DS3 Mode)

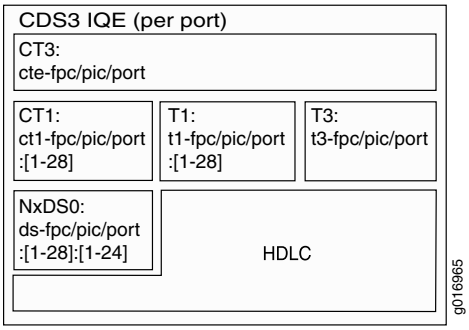

Figure 10: Channelized CDS3/E3 IQE PIC (in E3 Mode)

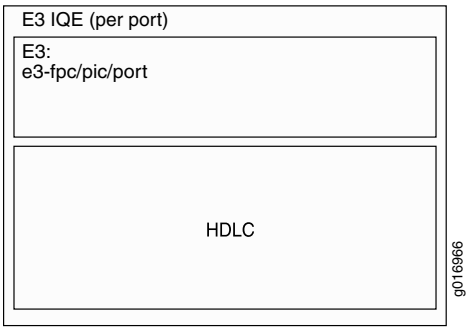

Figure 11: Channelized DS3 IQ PIC

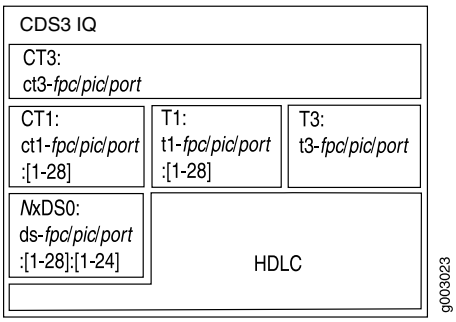

Figure 12: Channelized T1 IQ and IQE PIC

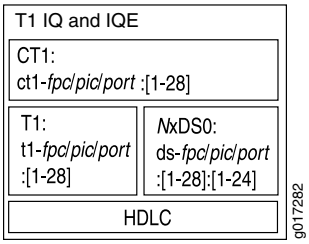

Figure 13: Channelized E1 IQ and IQE PIC

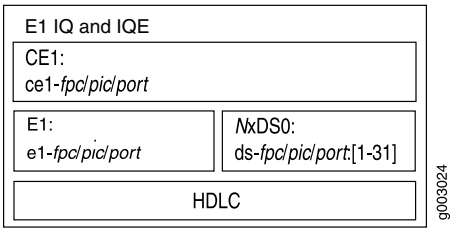

Table 1: Structural Differences: Channelized IQE PICs

PIC Type	Transport	Path	DS3	DS1/E1	E3
Channelized IQE PICs					
Channelized OC48/STM16 IQE (SONET Mode)	coc48-*fpc/pic/port*	coc1-*fpc/pic/port* :[1-48] so-*fpc/pic/port*	ct3-*fpc/pic/port* :[1-48] t3-*fpc/pic/port* :[1-48]	ct1-*fpc/pic/port* :[1-48]:[1-28] t1-*fpc/pic/port* :[1-48]:[1-28]	Not applicable.
Channelized OC48/STM16 IQE (SDH Mode)	cstm16-*fpc/pic/port*	cau4-*fpc/pic/port* :[1-16] so-*fpc/pic/port*	ct3-*fpc/pic/port* :[1:16][1:3] t3-*fpc/pic/port* :[1:16][1:3] ct1-*fpc/pic/port* :[1:16]:[1-84] t1-*fpc/pic/port* :[1:16]:[1-84]	ce1-*fpc/pic/port* :[1-16]:[1-63] e1-*fpc/pic/port* :[1-16]:[1-63] ct1-*fpc/pic/port* :[1:16]:[1-3]:[1-28] t1-*fpc/pic/port* :[1:16]:[1-3]:[1-28]	e3-*fpc/pic/port* :[1-16]:[1-3]
Channelized OC12 IQE (SONET Mode)	coc12-*fpc/pic/port*	coc1-*fpc/pic/port* :[1-12] so-*fpc/pic/port*	ct3-*fpc/pic/port* :[1-12] t3-*fpc/pic/port* :[1-12]	ct1-*fpc/pic/port* :[1-12]:[1-28] t1-*fpc/pic/port* :[1-12]:[1-28]	Not applicable.
Channelized STM4 IQE (SDH Mode)	cstm4-*fpc/pic/port*	cau4-*fpc/pic/port*:[1-4] so-*fpc/pic/port*	ct3-*fpc/pic/port* :[1-4]:[1–3] t3-*fpc/pic/port* :[1-4]:[1–3] ct1-*fpc/pic/port* :[1-4]:[1-84] t1-*fpc/pic/port* :[1–4]:[1-84]	ce1-*fpc/pic/port* :[1-4]:[1-63] e1-*fpc/pic/port* :[1-4]:[1-63] ct1-*fpc/pic/port* :[1-4]:[1–3]:[1-28] t1-*fpc/pic/port* :[1-4]:[1–3]:[1-28]	e3-*fpc/pic/port* :[1-4]:[1:3]
Channelized OC3 IQE (SONET)	coc3-*fpc/pic/port*	coc1-*fpc/pic/port* :[1-3] so-*fpc/pic/port*	ct3-*fpc/pic/port* :[1-3] t3-*fpc/pic/port* :[1-3]	ct1-*fpc/pic/port* :[1-3]:[1-28] t1-*fpc/pic/port* :[1-3]:[1-28]	Not applicable.
Channelized STM1 IQE	cstm1-*fpc/pic/port*	cau4-*fpc/pic/port* so-*fpc/pic/port*	ct3-*fpc/pic/port* :[1-3] t3-*fpc/pic/port* :[1-3] ct1-*fpc/pic/port* :[1-84] t1-*fpc/pic/port* :[1-84]	ce1-*fpc/pic/port* :[1-63] e1-*fpc/pic/port* :[1-63] ct1-*fpc/pic/port* :[1-3]:[1-28] t1-*fpc/pic/port* :[1-3]:[1-28]	e3-*fpc/pic/port* :[1:3]]

Table 1: Structural Differences: Channelized IQE PICs *(continued)*

PIC Type	Transport	Path	DS3	DS1/E1	E3
Channelized DS3 IQE	Not applicable.	Not applicable.	ct3-*fpc/pic/port* t3-*fpc/pic/port*	ct1-*fpc/pic/port* :[1-28] t1-*fpc/pic/port* :[1-28]	Not applicable.
Channelized E3 IQE	Not applicable.	Not applicable.	Not applicable.	Not applicable.	e3-*fpc/pic/port* :[1:4]
Channelized T1 IQE	Not applicable.	Not applicable.	Not applicable.	ct1-*fpc/pic/port* t1-*fpc/pic/port*	Not applicable.
Channelized E1 IQE	Not applicable.	Not applicable.	Not applicable.	ce1-*fpc/pic/port* e1-*fpc/pic/port*	Not applicable.

Table 2: Structural Differences: Channelized IQ PICs

PIC Type	Transport	Path	DS3	DS1/E1	E3
Channelized IQ PICs					
Channelized OC12/STM4 IQ (SONET Mode)	coc12-*fpc/pic/port*	coc1-*fpc/pic/port* :[1-12] so-*fpc/pic/port*	ct3-*fpc/pic/port* :[1-4]:[1-3] t3-*fpc/pic/port* :[1-4]:[1-3]	ct1-*fpc/pic/port* :[1-3]:[1-28] ct1-*fpc/pic/port* :[1-4]:[1-3]:[1-28]	Not applicable.
Channelized OC12/STM4 IQ (SDH Mode)	cstm4-*fpc/pic/port*	cau4-*fpc/pic/port*:[1-4] so-*fpc/pic/port*	ct3-*fpc/pic/port* :[1-4]:[1-3] t3-*fpc/pic/port* :[1-4]:[1-3]	ct1-*fpc/pic/port* :[1-3]:[1-28] t1-*fpc/pic/port* :[1-4]:[1-3]:[1-28]	Not applicable.
Channelized OC3 IQ (SONET)	coc3-*fpc/pic/port*	coc1-*fpc/pic/port* :[1-3] so-*fpc/pic/port*	ct3-*fpc/pic/port* :[1-3] t3-*fpc/pic/port* :[1-3]	ct1-*fpc/pic/port* :[1-3]:[1-28] t1-*fpc/pic/port* :[1-3]:[1-28]	Not applicable.
Channelized STM1 IQ (SDH)	Not applicable.	cau4-*fpc/pic/port* so-*fpc/pic/port*	Not applicable.	ce1-*fpc/pic/port* :[1-63] e1-*fpc/pic/port* :[1-63]	Not applicable.
Channelized DS3 IQ	Not applicable.	Not applicable.	ct3-*fpc/pic/port* t3-*fpc/pic/port*	ct1-*fpc/pic/port* :[1-28] t1-*fpc/pic/port* :[1-28]	Not applicable.

Table 2: Structural Differences: Channelized IQ PICs *(continued)*

PIC Type	Transport	Path	DS3	DS1/E1	E3
Channelized E1 IQ	Not applicable.	Not applicable.	Not applicable.	ce1-*fpc/pic/port* e1-*fpc/pic/port*	Not applicable.

Table 3: Structural Differences: Channelized PICs

PIC Type	Transport	Path	DS3	DS1/E1	E3
Channelized PICs					
Channelized OC12	t3-*fpc/pic/port* :0	t3-*fpc/pic/port* :[0-11]	t3-*fpc/pic/port* :[0-11]	Not applicable.	Not applicable.
Channelized STM1	e1-*fpc/pic/port* :0	e1-*fpc/pic/port* :0	Not applicable.	e1-*fpc/pic/port* :[0-63]	Not applicable.
Channelized T3 and Multichannel T3	Not applicable.	Not applicable.	t1-*fpc/pic/port* :0	t1-*fpc/pic/port* :[0-27]	Not applicable.
Channelized E1	Not applicable.	Not applicable.	Not applicable.	e1-*fpc/pic/port* ds-*fpc/pic/port* :0	Not applicable.

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