Data-Link Connection Identifiers on Channelized Interfaces

If you use Frame Relay encapsulation on a channelized interface, see Table 1 for the maximum number of data-link connection identifiers (DLCIs) per channel that you can configure at each channel level for various channelized PICs.

If you use a per-unit-scheduler configuration on a channelized interface, see Table 2 for the maximum number of data-link connection identifiers (DLCIs) per channel that you can configure at each channel level for various channelized PICs.

NOTE: The actual number of DLCIs you can configure for each channel is determined by the capabilities of your system, such as the number and types of PICs installed. If the number of DLCIs in the configuration exceeds the capabilities of your system, the router might not be able to support the maximum DLCI values shown in Table 1. To determine the capabilities of your system, please contact Juniper Networks customer support.

Table 1: Frame Relay DLCI Limitations for Channelized Interfaces

PIC Types	Number of DLCIs per Level	Range
Original Channelized PICs		
DS0 level channels	3 for sparse mode	1–1022 for sparse mode (0 is reserved for the Local Management Interface [LMI])
T3 and T1 level channels	63 for regular mode	1–63 for regular mode
	3 for sparse mode	1–1022 for sparse mode (0 is reserved for the LMI)
Channelized IQ and IQE PICs		
DS0 level channels (Channelized DS3 IQ or IQE, Channelized STM1 IQ or IQE, Channelized E1 IQ or IQE, Channelized OC3 IQ or IQE, or Channelized OC12 IQ or IQE PICs)	16	1–1022 (0 is reserved for the LMI)
E1 level channels (Channelized E1 IQ or IQE PIC)	64	1–1022 (0 is reserved for the LMI)
E1 level channels (Channelized STM1 IQ or IQE PIC)	64	1–1022 (0 is reserved for the LMI)
OC3 level channels (Channelized OC3 IQ or IQE, or Channelized OC12 IQ or IQE PIC)	1022	1–1022 (0 is reserved for the LMI)
OC12 level channels (Channelized OC12 IQ or IQE, Channelized OC48/STM16 IQE PICs, and (per port on) OC12 ports on 4xOC12/STM4 IQE PICs)	1022	1–1022 (0 is reserved for the LMI)
STM1 level channel (Channelized STM1 IQ or IQE PIC)	1022	1–1022 (0 is reserved for the LMI)

Table 1: Frame Relay DLCI Limitations for Channelized Interfaces *(continued)*

PIC Types	Number of DLCIs per Level	Range
T1 level channels (Channelized DS3 IQ or IQE PIC)	64	1–1022 (0 is reserved for the LMI)
T1 level channels (Channelized OC3 IQ or IQE, or Channelized OC12 IQ or IQE PIC)	64	1–1022 (0 is reserved for the LMI)
T3 level channel (Channelized DS3 IQ or IQE, Channelized OC3 IQ or IQE, or Channelized OC12 IQ or IQE PIC)	1022	1–1022 (0 is reserved for the LMI)

Table 2: Per Unit Scheduler DLCI Limitations for Channelized Interfaces

	Number of DLCIs per Level			
	Non M40e Platforms		M40e Platform Only	
PIC Types	With Per-Unit-Scheduler	Without Per-Unit-Scheduler	With Per-Unit-Scheduler	Without Per-Unit-Scheduler
DS0 level channels	64	64	16	16
T1/E1 level channels	64	64	64	64
DS3/E3 level channels	975	† Protocol family combinations apply	256	256
SONET	975	† Protocol family combinations apply	975	† Protocol family combinations apply

† In these router, PIC, and scheduler configurations, combining multiple protocol families per PIC changes the number of Frame Relay DLCIs as shown in Table 3.

Table 3: Protocol Family Combinations

Protocol Family Combinations	Number of DLCIs per PIC
inet	3600
inet6	3600
mpls	3000
inet, inet6	2400
inet, mpls	2000
inet6, mpls	2000

Table 3: Protocol Family Combinations *(continued)*

Protocol Family Combinations	Number of DLCIs per PIC
inet, inet6, mpls	1550

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