# Letter of Volatility - CTP150

The table below identifies all the memory locations in the CTP150 product. This includes the CTP150 processor and the CTP150 T1E1 and Serial modules. All customer data (payload) is only stored in the FPGA, System RAM, packet memory, PCI controllers, and Ethernet controllers. All of these locations are transient and volatile. All the contents in these locations will be deleted when the power is turned off on the system. The term User Data in the table below includes node and network configuration data. That data is not customer [payload] data. The procedure for sanitization of User Data is identified in the table below.

| CTP150 Chassis + Processor | Part # | Device | Memory Size | Type | Volatility | User Data | Purpose | Sanitization Procedure |
|---|---|---|---|---|---|---|---|---|
| CTP150-AC | 740-032793 | Main Memory | 1024MB | DDR2 SDRAM | Volatile | Yes | System Memory | Power down system |
| CTP150-AC | 740-032793 | CPU L1 Cache | 64KB | SRAM | Volatile | Yes | Level one cache | Power down system |
| CTP150-AC | 740-032793 | CPU L2 Cache | 512KB | SRAM | Volatile | Yes | Level two cache | Power down system |
| CTP150-AC | 740-032793 | Firmware memory | 2Mbit | Flash PROM | Non-Volatile | No | Holds BIOS | N/A |
| CTP150-AC | 740-032793 | CMOS Memory | < 1K bytes | Battery backed SRAM | Non-Volatile when battery is fitted | Yes | Holds the time and date plus the BIOS configuration parameters | Remove battery |
| CTP150-AC | 740-032793 | ICH9 (SouthBridge) | < 8MB | SRAM | Volatile | Yes | Graphics/SATA/PCIe/GigE buffers/registers | Power down system |

 

| CTP150 Chassis + Processor | Part # | Device | Memory Size | Type | Volatility | User Data | Purpose | Sanitization Procedure |
|---|---|---|---|---|---|---|---|---|
| CTP150-IM-T1E1 | 710-033780 | U42 (Personality EEPROM) | 256 x 8 bits | Serial EEPROM | Non-Volatile | Yes | Storage for card serial numbers, calibration data, etc… | CTPOS PCB description edit (Node Test Menu) |
| CTP150-IM-T1E1 | 710-033780 | U49 (Main FPGA) | 16,951,824 bits FPGA Configuration RAM + 2,475,072 bits FPGA User RAM + Logic Registers | SRAM-Based FPGA | Volatile | Yes | FPGA for data/packet/clock generation and routing | Power down system |
| CTP150-IM-T1E1 | 710-033780 | U2 (DDR Memory) | 128M x 8 bits | DDR II SDRAM | Volatile | No | Currently unused by system | Power down system |
| CTP150-IM-T1E1 | 710-033780 | U4 (T1E1 Framer/LIU) | < 1MB | SRAM | Volatile | Yes | Internal regsister and T1E1 payload frame buffers | Power down system |
| CTP150-IM-T1E1 | 710-033780 | U33 (Security Chip) | 18 KB EEPROM + 112 KB ROM + 4 KB RAM | EEPROM/ROM/RAM | Non-Volatile | No | Security (Anti Counterfeit) Device | N/A |
| CTP150-IM-T1E1 | 710-033780 | U41 (FPGA config Flash) | 67,108,864 bits FPGA configuration FLASH | Serial Flash | Non-Volatile | No | FPGA image storage (2 images) | N/A |

 

| CTP150 Chassis + Processor | Part # | Device | Memory Size | Type | Volatility | User Data | Purpose | Sanitization Procedure |
|---|---|---|---|---|---|---|---|---|
| CTP150-IM-SER | 710-033781 | U55 (Personality EEPROM) | 256 x 8 bits | Serial EEPROM | Non-Volatile | Yes | Storage for card serial numbers, calibration data, etc… | CTPOS PCB description edit (Node Test Menu) |
| CTP150-IM-SER | 710-033781 | U43 (Main FPGA) | 16,951,824 bits FPGA Configuration RAM + 2,475,072 bits FPGA User RAM + Logic Registers | SRAM-Based FPGA | Volatile | Yes | FPGA for data/packet/clock generation and routing | Power down system |
| CTP150-IM-SER | 710-033781 | U44 (DDR Memory) | 128M x 8 bits | DDR II SDRAM | Volatile | No | Currently unused by system | Power down system |
| CTP150-IM-SER | 710-033781 | U33 (Security Chip) | 18 KB EEPROM + 112 KB ROM + 4 KB RAM | EEPROM/ROM/RAM | Non-Volatile | No | Security (Anti Counterfeit) Device | N/A |
| CTP150-IM-SER | 710-033781 | U64 (FPGA config Flash) | 67,108,864 bits FPGA configuration FLASH | Serial Flash | Non-Volatile | No | FPGA image storage (2 images) | N/A |

 