

M160 Internet Router

PIC Guide

End-of-Life PICs

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Part Number: 530-009717-01, Revision 5

This guide provides an overview and description of the Physical Interface Cards (PICs) supported by the Juniper Networks M160 Internet router that are end-of-life and can no longer be ordered. The PICs are described alphabetically.

PICs provide the physical connection to various network media types. The PICs are mounted on Flexible PIC Concentrators (FPCs) or Enhanced Flexible PIC Concentrator (Enhanced FPCs), which are inserted into a slot in a router. A PIC occupies a single slot on an FPC. You can install PICs of different media types on the same FPC as long as the FPC and the router support those PICs.

PICs receive incoming packets from the network and transmit outgoing packets to the network. During this process, each PIC performs framing and high-speed signaling for its media type. Before transmitting outgoing data packets, the PICs encapsulate the packets received from the FPCs. Each PIC is equipped with a media-specific ASIC that performs control functions tailored to the PIC's media type.



NOTE: A single FPC2 has a maximum throughput of 10 Gbps and a single FPC1 has a maximum throughput of 3.2 Gbps. Inserting a combination of PICs with an aggregate higher than that is supported, but constitutes oversubscription.

You can typically install any combination of PICs on a single Enhanced Flexible PIC Concentrator (FPC). Starting with JUNOS Release 6.2, on M5, M10, M20, M40, M40e, and M160 routers, there are some combinations of PICs that cannot be installed together on the same Enhanced FPC. If you are adding a new type of PIC to an existing configuration, see the *PIC Combination Notes Summary* CS technical bulletin (ID number PSN-2004-12-002) at <http://www.juniper.net/alerts>.

Blank PICs resemble other PICs, but do not provide any physical connection or activity. When a slot is not occupied by a PIC, you must insert a blank PIC to fill the empty slot and ensure proper cooling of the system.

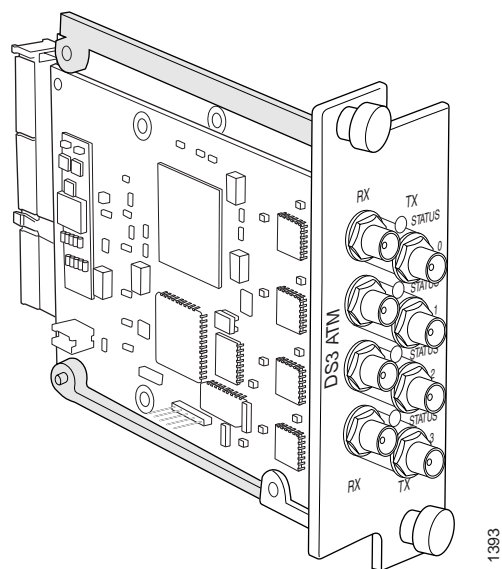
For complete information about installing PICs, including installation of small form-factor pluggable transceivers (SFPs), refer to the *PIC, SFP, and XENPAK Installation Instructions* located at <http://www.juniper.net/techpubs/>.

Table 1 lists the PICs supported by the M160 Internet router.

Table 1: End-of-Life PICs Supported in the M160 Internet Router

PIC Family and Type	Ports	First JUNOS Support	FPC Support and PIC Slots Required	Page
ATM				
ATM DS3	4	4.3	FPC1—1 slot	4
ATM E3	4	4.3	FPC1—1 slot	6
ATM OC3	2	4.0	FPC1—1 slot	8
ATM OC12	1	4.0	FPC1—1 slot	11
Channelized				
Channelized DS3	4	4.2	FPC1—1 slot	14
Channelized E1	10	5.4	FPC1—1 slot	16
Channelized STM1 to E1	1	4.4R3	FPC1—1 slot	18
E3				
E3	4	4.1	FPC1—1 slot	20
Ethernet				
Gigabit Ethernet	1	4.0	FPC1—1 slot	22
Gigabit Ethernet	2	4.1	FPC2—1 slot	22
Gigabit Ethernet	4	5.0	FPC2—1 slot	22
SONET/SDH				
SONET/SDH OC48c/STM16	1	4.0	FPC2—1 slot	25

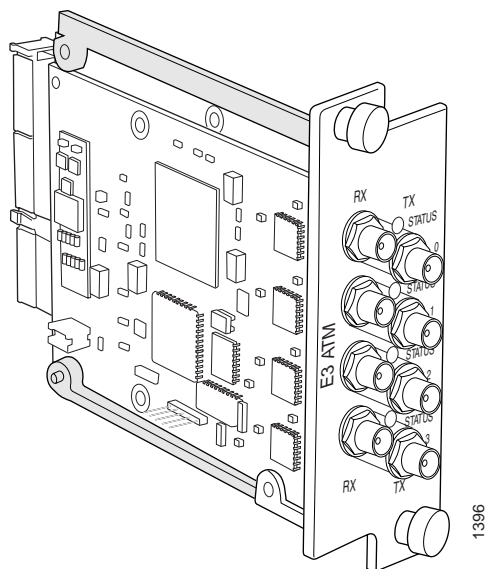
ATM DS3 PIC



Software release	■ JUNOS 4.3 and later
Description	<div>■ Four DS3 ports</div> <div>■ Power requirements: 0.39 A/48 V @ 19.0 W</div> <div>■ Conforms to ANSI T1.105-1991 and T1E1.2/93-020R1</div> <div>■ Asynchronous Transfer Mode (ATM) standards compliant</div> <div>■ Alarm and event counting and detection</div> <div>■ Compatible with well-known ATM switches</div> <div>■ ATM switch ID, which displays the switch IP address and local interface name of the adjacent Fore ATM switches</div>
Hardware features	<div>■ OAM fault management processes Alarm Indication Signal (AIS) and Remote Defect Indicator (RDI) cells</div> <div>■ ASIC-based packet segmentation and reassembly (SAR) management and output port queuing</div> <div>■ 16-MB SDRAM memory for ATM SAR</div> <div>■ Packet buffering, Layer 2 parsing</div> <div>■ Configurable framing options:<div>■ C-bit with ATM direct mapping</div><div>■ C-bit with PLCP framing (default)</div><div>■ M23 ATM direct mapping</div><div>■ M23 with PLCP framing</div></div>

Software features	<ul style="list-style-type: none"> ■ Multiprotocol Label Switching (MPLS) circuit cross-connect (CCC) for leveraging ATM access networks ■ Support for user-configurable virtual circuits (VC) and virtual paths (VP) ■ ATM Inverse Address Resolution Protocol (ARP), which enables routers to automatically learn the IP address of the router on the far end of an ATM permanent virtual circuit (PVC) ■ Unspecified bit rate (UBR) traffic shaping ■ Fine-grained variable bit rate (VBR) traffic shaping ■ Outbound PIC queues cells on a per-VC basis ■ Encapsulations—AAL5 subnetwork attachment point (SNAP)
Cables and connectors	<ul style="list-style-type: none"> ■ 10-ft (3.05-m) posilock SMB to BNC ■ Four pairs of RX and TX coaxial cables
LEDs	<p>One tricolor per port:</p> <ul style="list-style-type: none"> ■ Off—Not enabled ■ Green—Online with no alarms or failures ■ Amber—Online with alarms for remote failures ■ Red—Active with a local alarm; router has detected a failure
Alarms, errors, and events	<ul style="list-style-type: none"> ■ Alarm Indication Signal (AIS) ■ Far-end Block Error (FEBE) ■ Frame Error ■ Idle code ■ Idle received ■ Local and remote loopback ■ Loss of Signal (LoS) ■ Out of Frame (OoF) ■ Path parity error ■ Yellow alarm

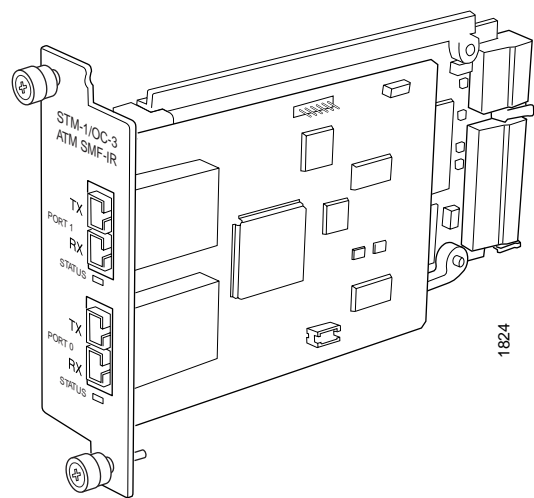
ATM E3 PIC



Software release	<ul style="list-style-type: none">■ JUNOS 4.3 and later
Description	<ul style="list-style-type: none">■ Four E3 ports■ Power requirements: 0.43 A/48 V @ 20.8 W■ Conforms to ANSI T1.105-1991 and T1E1.2/93-020R1■ Asynchronous Transfer Mode (ATM) standards compliant■ Alarm and event counting and detection■ Compatible with well-known ATM switches■ ATM switch ID, which displays the switch IP address and local interface name of the adjacent Fore ATM switches
Hardware features	<ul style="list-style-type: none">■ OAM fault management processes Alarm Indication Signal (AIS) and Remote Defect Indicator (RDI) cells■ ASIC-based packet segmentation and reassembly (SAR) management and output port queuing■ 16-MB SDRAM memory for ATM SAR■ Packet buffering, Layer 2 parsing■ Configurable framing options:<ul style="list-style-type: none">■ G.751 direct mapping■ G.751 with PLCP encapsulation (default)■ G.832 ATM direct mapping

Software features	<ul style="list-style-type: none"> ■ Multiprotocol Label Switching (MPLS) circuit cross-connect (CCC) for leveraging ATM access networks ■ Support for user-configurable virtual circuits (VC) and virtual paths (VP) ■ ATM Inverse Address Resolution Protocol (ARP), which enables routers to automatically learn the IP address of the router on the far end of an ATM permanent virtual circuit (PVC) ■ Unspecified bit rate (UBR) traffic shaping ■ Fine-grained variable bit rate (VBR) traffic shaping ■ Outbound PIC queues cells on a per-VC basis ■ Encapsulations—AAL5 subnetwork attachment point (SNAP)
Cables and connectors	<ul style="list-style-type: none"> ■ 10-ft (3.05-m) posilock SMB to BNC ■ Four pairs of RX and TX coaxial cables
LEDs	<p>One tricolor per port:</p> <ul style="list-style-type: none"> ■ Off—Not enabled ■ Green—Online with no alarms or failures ■ Amber—Online with alarms for remote failures ■ Red—Active with a local alarm; router has detected a failure
Alarms, errors, and events	<ul style="list-style-type: none"> ■ Alarm Indication Signal (AIS) ■ Frame Error ■ Line code violation ■ Local and remote loopback ■ Loss of Signal (LoS) ■ Out of Frame (OoF) ■ Yellow alarm

ATM OC3 PIC



Software release	<ul style="list-style-type: none">JUNOS 4.0 and later
Description	<ul style="list-style-type: none">Two OC3 portsPower requirements: 0.49 A/48 V @ 23.7 WConforms to ANSI T1.105-1991 and T1E1.2/93-020R1ATM and SONET/SDH standards compliantAlarm and event counting and detectionCompatible with well-known ATM switchesATM switch ID, which displays the switch IP address and local interface name of the adjacent Fore ATM switchesOptical interface support—see Table 2
Hardware features	<ul style="list-style-type: none">Dual 3010 SAR for segmentation and reassembly into 53-byte ATM cellsHigh-performance parsing of SONET/SDH framesOAM fault management processes Alarm Indication Signal (AIS) and Remote Defect Indicator (RDI) cellsASIC-based packet segmentation and reassembly (SAR) management and output port queuing16-MB SDRAM memory for ATM SARPacket buffering, Layer 2 parsing

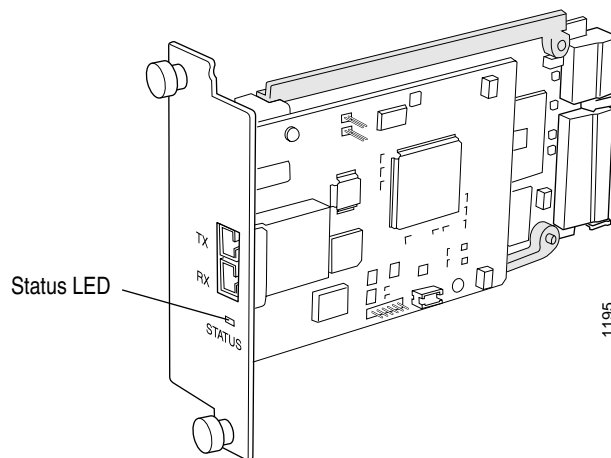
Software features	<ul style="list-style-type: none"> ■ Multiprotocol Label Switching (MPLS) circuit cross-connect (CCC) for leveraging ATM access networks ■ Support for user-configurable virtual circuits (VC) and virtual paths (VP) ■ ATM Inverse Address Resolution Protocol (ARP), which enables routers to automatically learn the IP address of the router on the far end of an ATM permanent virtual circuit (PVC) ■ Unspecified bit rate (UBR) traffic shaping ■ Fine-grained variable bit rate (VBR) traffic shaping ■ Outbound PIC queues cells on a per-VC basis ■ Encapsulations—AAL5 subnetwork attachment point (SNAP)
Cables and connectors	<ul style="list-style-type: none"> ■ Duplex SC/PC connector (RX and TX)
LEDs	<p>One tricolor per port:</p> <ul style="list-style-type: none"> ■ Off—Not enabled ■ Green—Online with no alarms or failures ■ Amber—Online with alarms for remote failures ■ Red—Active with a local alarm; router has detected a failure
Alarms, errors, and events	<ul style="list-style-type: none"> ■ Alarm Indication Signal (AIS-L, AIS-P) ■ Bit Error Rate Signal Degrade (BERR-SD), Bit Error Rate Signal Fail (BERR-SF) ■ Bit Interleaved Parity Errors B1, B2, B3 (CV-S, CV-L, CV-P) ■ Errored Seconds (ES-S, ES-L, ES-P), Far-end Bit Errors REI-L, REI-P (CV-LFE, CV-PFE), Far-end Errored Seconds (ES-LFE, ES-PFE), Far-end Severely Errored Seconds (SES-LFE, SES-PFE), Far-end Unavailable Seconds (UAS-LFE, UAS-PFE) ■ Loss of Cell Delineation (LoC), Loss of Frame (LoF), Loss of Pointer (LoP-P), Loss of Signal (LoS) ■ Payload Mismatch (PLM-P), Payload Unequipped (UNEQ-P) ■ Remote Defect Indication (RDI-L, RDI-P) ■ Severely Errored Framing (SEF), Severely Errored Framing Seconds (SEFS-S), Severely Errored Seconds (SES-S, SES-L, SES-P), Unavailable Seconds (UAS-L, UAS-P)

Table 2: Optical Interface Support for ATM OC3 PICs

PIC Type	Single-mode Intermediate Reach	Multimode
Optical interface	Single-mode, intermediate reach (Bellcore GR-253 compliant) with SC/PC duplex connector (maximum distance 9.3 miles/15 km)	Multimode with SC/PC duplex connector (maximum distance 1.2 miles/2 km), ATM Forum af-phy-0046
Wavelength	1260 through 1360 nm	1270 through 1380 nm

PIC Type	Single-mode Intermediate Reach	Multimode
Average launch power	–15 through –8 dBm	–20 through –14 dBm
Receiver saturation	–8 dBm	–14 dBm
Receiver sensitivity	–28 dBm	–30 dBm

ATM OC12 PIC



Software release	<ul style="list-style-type: none"> ■ JUNOS 4.0 and later
Description	<ul style="list-style-type: none"> ■ One OC12 port ■ Power requirements: 0.43 A/48 V @ 20.8 W ■ Conforms to ANSI T1.105-1991 and T1E1.2/93-020R1 ■ ATM and SONET/SDH standards compliant ■ Alarm and event counting and detection ■ Compatible with well-known ATM switches ■ ATM switch ID, which displays the switch IP address and local interface name of the adjacent Fore ATM switches ■ Optical interface support—see Table 3
Hardware features	<ul style="list-style-type: none"> ■ High-performance parsing of SONET/SDH frames ■ OAM fault management processes Alarm Indication Signal (AIS) and Remote Defect Indicator (RDI) cells ■ ASIC-based packet segmentation and reassembly (SAR) management and output port queuing ■ 16-MB SDRAM memory for ATM SAR ■ Packet buffering, Layer 2 parsing

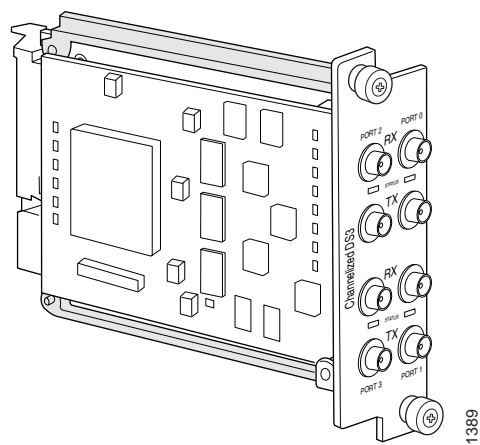
Software features	<ul style="list-style-type: none"> ■ Multiprotocol Label Switching (MPLS) circuit cross-connect (CCC) for leveraging ATM access networks ■ Support for user-configurable virtual circuits (VC) and virtual paths (VP) ■ ATM Inverse Address Resolution Protocol (ARP), which enables routers to automatically learn the IP address of the router on the far end of an ATM permanent virtual circuit (PVC) ■ Unspecified bit rate (UBR) traffic shaping ■ Fine-grained variable bit rate (VBR) traffic shaping ■ Outbound PIC queues cells on a per-VC basis ■ Encapsulations—AAL5 subnetwork attachment point (SNAP)
Cables and connectors	<ul style="list-style-type: none"> ■ Duplex SC/PC connector (RX and TX)
LEDs	<p>One tricolor per port:</p> <ul style="list-style-type: none"> ■ Off—Not enabled ■ Green—Online with no alarms or failures ■ Amber—Online with alarms for remote failures ■ Red—Active with a local alarm; router has detected a failure
Alarms, errors, and events	<ul style="list-style-type: none"> ■ Alarm Indication Signal (AIS-L, AIS-P) ■ Bit Error Rate Signal Degrade (BERR-SD), Bit Error Rate Signal Fail (BERR-SF) ■ Bit Interleaved Parity Errors B1, B2, B3 (CV-S, CV-L, CV-P) ■ Errored Seconds (ES-S, ES-L, ES-P), Far-end Bit Errors REI-L, REI-P (CV-LFE, CV-PFE), Far-end Errored Seconds (ES-LFE, ES-PFE), Far-end Severely Errored Seconds (SES-LFE, SES-PFE), Far-end Unavailable Seconds (UAS-LFE, UAS-PFE) ■ Loss of Cell Delineation (LoC), Loss of Frame (LoF), Loss of Pointer (LoP-P), Loss of Signal (LoS) ■ Payload Mismatch (PLM-P), Payload Unequipped (UNEQ-P) ■ Remote Defect Indication (RDI-L, RDI-P) ■ Severely Errored Framing (SEF), Severely Errored Framing Seconds (SEFS-S), Severely Errored Seconds (SES-S, SES-L, SES-P), Unavailable Seconds (UAS-L, UAS-P)

Table 3: Optical Interface Support for ATM OC12 PICs

PIC Type	Single-mode Intermediate Reach	Multimode
Optical interface	Single-mode, intermediate reach (Bellcore GR-253 compliant) with SC/PC duplex connector (maximum distance 9.3 miles/15 km)	Multimode with SC/PC duplex connector (maximum distance 546.8 yards/500 m), ATM Forum af-phy-0046
Wavelength	1274 through 1356 nm	1270 through 1380 nm

PIC Type	Single-mode Intermediate Reach	Multimode
Average launch power	–15 through –8 dBm	–20 through –14 dBm
Receiver saturation	–8 dBm	–14 dBm
Receiver sensitivity	–28 dBm	–26 dBm

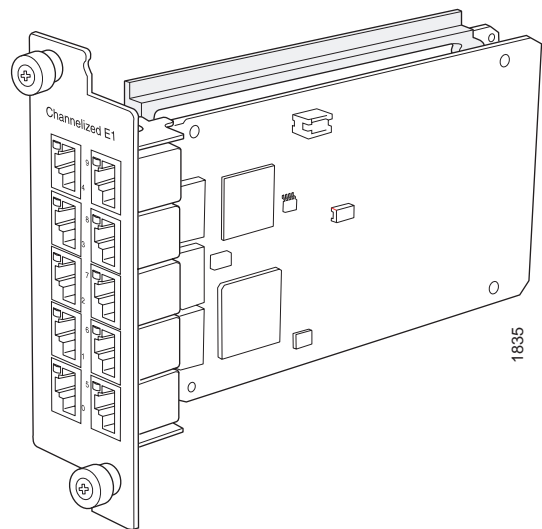
Channelized DS3 PIC



Software release	<ul style="list-style-type: none">■ JUNOS 4.2 and later
Description	<ul style="list-style-type: none">■ Four DS3 ports■ Power requirement: 0.32 A/48 V @ 15.6 W■ Supports up to 28 T1 channels per port■ Data Service Unit (DSU) functionality
Hardware features	<ul style="list-style-type: none">■ Each T1 channel supports a single High-level Data Link Control (HDLC) framer that can be configured for speeds ranging from DS0 (64 Kbps) through full T1 (1.54 Mbps)■ Predictable throughput on all ports at 1.54 Mbps, full duplex■ Rate limiting on input and output■ Packet buffering, Layer 2 parsing

Software features	<ul style="list-style-type: none"> ■ DS3 alarm and event counting ■ DS3 alarm and event detection ■ DS3 diagnostics and loopback control ■ B3ZS line encoding ■ M13 or C-bit parity ■ DS3 Simple Network Management Protocol (SNMP) support (DS3 MIB) ■ Per-packet counts and byte counts ■ Local and remote loopback testing ■ Encapsulations: <ul style="list-style-type: none"> ■ High-level Data Link Control (HDLC) ■ Frame Relay ■ Multiprotocol Label Switching (MPLS) circuit cross-connect (CCC) ■ Point-to-Point Protocol (PPP)
Cables and connectors	<ul style="list-style-type: none"> ■ Custom 10-ft (3.05-m) posilock to BNC male cable, separate RX and TX
LEDs	<p data-bbox="493 873 704 894">One tricolor per port:</p> <ul style="list-style-type: none"> ■ Off—Not enabled ■ Green—Online with no alarms or failures ■ Amber—Online with alarms for remote failures ■ Red—Active with a local alarm; router has detected a failure
Alarms, errors, and events	<ul style="list-style-type: none"> ■ Alarm Indication Signal (AIS) ■ Bit error rate (BER) ■ Equipment failure (Does not affect service) ■ Excessive zeros (EXZ) ■ Far-end Block Error (FEBE) ■ Frame error ■ Idle code, Idle received ■ Line code violation (LCV) ■ Local and remote loopback ■ Loss of Signal (LOS) ■ Out of Frame (OOF) ■ Parity bit (P-bit) disagreements ■ Path parity error ■ Yellow alarm bit (X-bit) disagreements

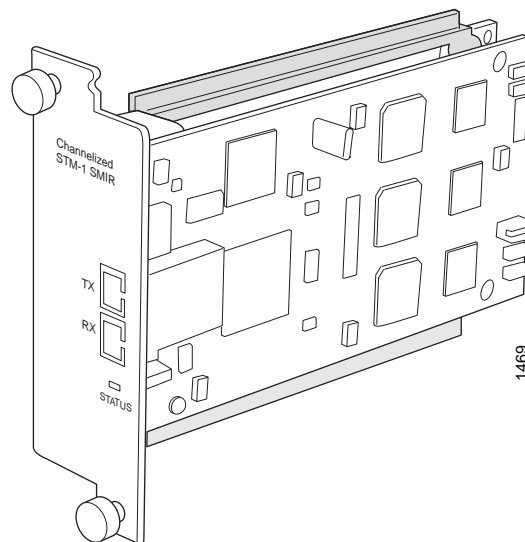
Channelized E1 PIC



Software release	■ JUNOS 5.4 and later
Description	<div>■ Ten E1 ports</div> <div>■ Power requirement: 0.15 A/48 V @ 7.2 W</div> <div>■ Supports up to 24 NxDS0 channels per port</div> <div>■ Data Service Unit (DSU) functionality</div>
Hardware features	<div>■ Ports configurable as clear channel E1 interfaces with 2.048-Mbps connectivity</div> <div>■ Rate limiting on input and output</div> <div>■ Packet buffering, Layer 2 parsing</div>
Software features	<div>■ Four data-link connection identifiers (DLCIs) per logical customer channel</div> <div>■ Unframed E1 G.703 and G.704 framing modes</div> <div>■ HDB3 line coding</div> <div>■ CRC4 configurable</div> <div>■ Per-packet counts and byte counts</div> <div>■ Local and remote loopback testing</div> <div>■ Encapsulations:<div><div>■ High-level Data Link Control (HDLC)</div><div>■ Frame Relay</div><div>■ Multiprotocol Label Switching (MPLS) circuit cross-connect (CCC)</div><div>■ Point-to-Point Protocol (PPP)</div></div></div>
Cables and connectors	■ 128-ohm RJ-48C

LEDs	One bicolor per port:
	<ul style="list-style-type: none">■ Off—Port not enabled■ Green—Physical E1 link is up; individual subchannels can be down■ Red—Physical E1 link is down
Alarms, errors, and events	<ul style="list-style-type: none">■ Alarm Indication Signal (AIS)■ Loss of Frame (LoF)■ Out of Frame (OoF)■ Failed Signal Rate (FSR)

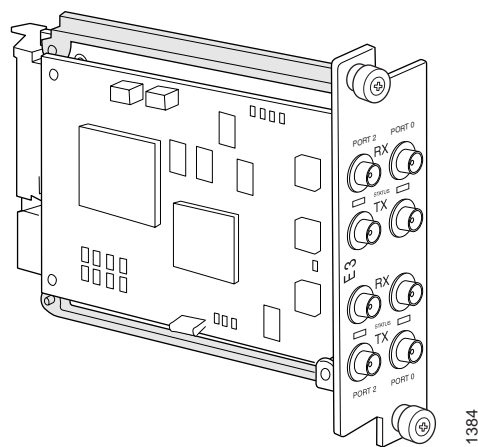
Channelized STM1 to E1 PIC



Software release	<ul style="list-style-type: none"> JUNOS 4.4R3 and later
Description	<ul style="list-style-type: none"> Four E3 ports Power requirement: 0.32 A/48 V @ 15.3 W 63 E1 channels
Hardware features	<ul style="list-style-type: none"> Each E1 channel supports a single High-level Data Link Control (HDLC) framer that can be configured for speeds from DS0 (64 Kbps) through full E1 (2 Mbps) in 64-Kbps increments Onboard DSU functionality for E1 and fractional E1 connectivity Integrated support for G.703 and unframed mode and G.704 framed mode with CRC; this feature is user-configurable Configurable clock source: Internal or loop Per-port loop timing Rate limiting on input and output NxE1 service with Multilink Point-to-Point Protocol (MLPPP, RFC 1990) delivered by the Link Services and Multilink Services PICs

Software features	<ul style="list-style-type: none"> ■ SDH mapping: <ul style="list-style-type: none"> ■ Tributary Unit Group 3 (TUG-3) ■ E1 support: <ul style="list-style-type: none"> ■ Full instrumentation per E1 channel ■ Integrated support for G.703 unframed mode and G.704 framed mode ■ 4-bit CRC for G.704 framed mode ■ HDB3 coding ■ Local E1 line loopback and remote line loopback ■ Per-channel BERT testing ■ Encapsulations: <ul style="list-style-type: none"> ■ Cisco High-level Data Link Control (HDLC) ■ Frame Relay ■ Multiprotocol Label Switching (MPLS) circuit cross-connect (CCC) ■ MPLS translational cross-connect (TCC) ■ Point-to-Point Protocol (PPP)
Cables and connectors	<ul style="list-style-type: none"> ■ Single-mode fiber ■ Duplex SC/PC connector (RX and TX)
LEDs	<p>One tricolor per port:</p> <ul style="list-style-type: none"> ■ Off—Not enabled ■ Green—Online with no alarms or failures ■ Amber—Online with alarms for remote failures ■ Red—Active with a local alarm; router has detected a failure
Alarms, errors, and events	<ul style="list-style-type: none"> ■ Alarm Indication Signal (AIS) ■ Bit Error Rate Signal Degrade (BERR-SD), Bit Error Rate Signal Fail (BERR-SF) ■ Bit Error Rate Testing (BERT) per E1 channel ■ Bit Interleaved Parity Errors B1, B2, B3 (CV-S, CV-L, CV-P) ■ Loss of Frame (LoF), Loss of Pointer (LoP-P), Loss of Signal (LoS) ■ Payload Mismatch (PLM-P), Payload Unequipped (UNEQ-P) ■ Remote Defect Indication (RDI-L, RDI-P) ■ Errored Seconds (ES-S, ES-L, ES-P), Severely Errored Framing (SEF), Severely Errored Framing Seconds (SEFS-S), Severely Errored Seconds (SES-S, SES-L, SES-P), Unavailable Seconds (UAS-L, UAS-P) ■ Yellow alarm bit (X-bit) disagreements

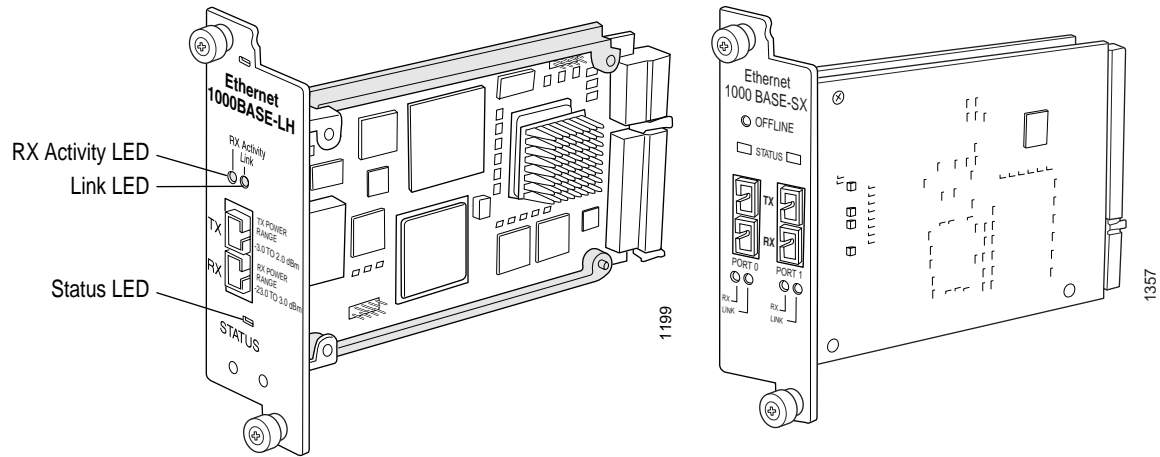
E3 PIC



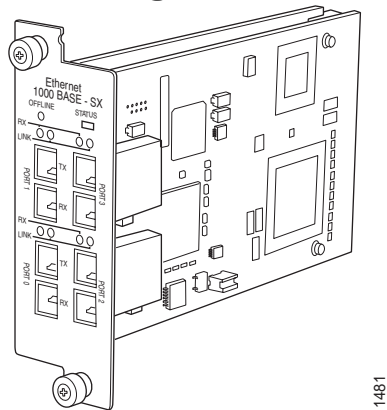
Software release	<ul style="list-style-type: none">JUNOS 4.1 and later
Description	<ul style="list-style-type: none">Four E3 portsPower requirement: 0.47 A/48 V @ 22.5 WIntegrated DSU interoperability
Hardware features	<ul style="list-style-type: none">High-density E3 (34.368-Mbps) connectivityHigh-performance throughput on all ports at speeds up to 34.368 Mbps, full duplexScrambling supportSubrate clocking supportRate policing on inputRate shaping on outputPacket buffering, Layer 2 parsingLarge MTUs, up to 9192 bytesLocal and remote loopback

Software features	<ul style="list-style-type: none"> ■ Supports G-751 framing ■ E3 diagnostics and loopback control ■ E3 alarm and event counting and detection ■ DS3 diagnostics and loopback control ■ Bit Error Rate Test (BERT); you can configure one port in BERT mode and configure the remaining channels to transmit and receive normal traffic ■ Encapsulations: <ul style="list-style-type: none"> ■ High-level Data Link Control (HDLC) ■ Frame Relay ■ Multiprotocol Label Switching (MPLS) circuit cross-connect (CCC) ■ Point-to-Point Protocol (PPP)
Cables and connectors	<ul style="list-style-type: none"> ■ Custom 10-ft (3.05-m) posilock to BNC male cable, separate RX and TX
LEDs	<p data-bbox="492 751 703 772">One tricolor per port:</p> <ul style="list-style-type: none"> ■ Off—Not enabled ■ Green—Online with no alarms or failures ■ Amber—Online with alarms for remote failures ■ Red—Active with a local alarm; router has detected a failure
Alarms, errors, and events	<ul style="list-style-type: none"> ■ Alarm Indication Signal (AIS) ■ Equipment failure (does not affect service) ■ Frame error ■ Line code violation ■ Loss of Signal (LoS) ■ Out of Frame (OoF) ■ Yellow alarm bit (A-bit) disagreements

Gigabit Ethernet PICs



Left: 1-Port Gigabit Ethernet; Right: 2-Port Gigabit Ethernet



4-Port Gigabit Ethernet

Software release

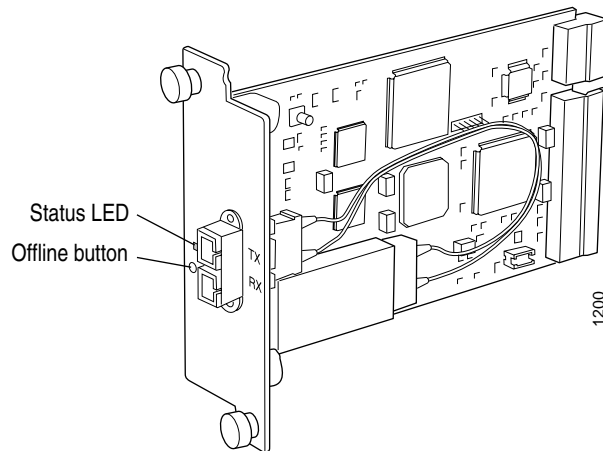
- 1-port: JUNOS 4.0 and later
- 2-port: JUNOS 4.1 and later
- 4-port: JUNOS 5.0 and later

Description	<ul style="list-style-type: none"> ■ One, two, or four Gigabit Ethernet ports ■ Power requirements: <ul style="list-style-type: none"> ■ 1-port: 0.27 A/48 V @ 13.2 W ■ 2-port: 0.35 A/48 V @ 17 W ■ 4-port: 0.40 A/48 V @ 19.2 W ■ Supports large Ethernet frame sizes for more efficient throughput across the intra-POP network ■ Optical interface support—see Table 4
Hardware features	<ul style="list-style-type: none"> ■ High-performance throughput on all ports at speeds up to 1 Gbps ■ Autonegotiation between Gigabit Ethernet circuit partners ■ Full-duplex mode ■ Maximum transmission units (MTUs) of up to 9192 bytes <p>Note: If you use a 4-port Gigabit Ethernet PIC on a Juniper Networks M160 router, the MTU will decrease to 4500 bytes.</p>
Software features	<ul style="list-style-type: none"> ■ Virtual Router Redundancy Protocol (VRRP) support ■ 802.1Q virtual LANs (VLANs) support ■ 64 source MAC address filters per port ■ 960 destination MAC filters per port
Cables and connectors	<ul style="list-style-type: none"> ■ Duplex SC/PC connector (TX and RX)
LEDs	<p>Status LEDs, one bicolor:</p> <ul style="list-style-type: none"> ■ Off—PIC not enabled ■ Green—PIC is operating normally ■ Red—PIC has an error or failure <p>Port LEDs, one pair per port:</p> <ul style="list-style-type: none"> ■ Link—If green, the port is online; if there is no light, the port is down ■ Activity—If flashing green, the port is receiving data; if there is no light, the port might be on, but is not receiving data

Table 4: Optical Interface Support for Gigabit Ethernet PICs

PIC Type	SX Transceiver	LX Transceiver	LH Transceiver
Optical interface	656-ft/200-m reach on 62.5/125 micrometer multimode fiber (MMF) 1640-ft/500-m reach on 50/125 micrometer MMF	6.2-mile/10-km reach on 9/125 micrometer single-mode fiber (SMF) 1804.5-ft/550-m reach on 62.5/125 and 50/125 micrometer MMF	49.5-mile/70-km reach on 9/125 micrometer SMF
Wavelength	830 through 860 nm	1270 through 1355 nm	1480 through 1580 nm
Average launch power	–9.5 through –4 dBm	–11 through –3 dBm	–3 through +2 dBm
Receiver saturation	–3 dBm	–3 dBm	–3 dBm
Receiver sensitivity	–17 dBm	–19 dBm	–23 dBm (BER 10 ^{–12}) for SMF

SONET/SDH OC48c/STM16 PIC



Software release	<ul style="list-style-type: none"> ■ JUNOS 4.0 and later
Description	<ul style="list-style-type: none"> ■ One OC48 port ■ Power requirements: 0.38 A/48 V @ 18 W ■ Optical interface support—see Table 5 <p>NOTE: On the M5, M10, M20, M40, and M160 routers, this PIC requires an enhanced FPC. See the hardware guide for your router for more information.</p>
Hardware features	<ul style="list-style-type: none"> ■ Multiplexing and demultiplexing ■ Rate policing on input ■ Rate shaping on output ■ Packet buffering, Layer 2 parsing
Software features	<ul style="list-style-type: none"> ■ SONET/SDH framing ■ Alarm and event counting and detection ■ Dual-router automatic protection switching (APS) ■ Multiprotocol Label Switching (MPLS) fast reroute ■ Link aggregation ■ Encapsulations: <ul style="list-style-type: none"> ■ High-level Data Link Control (HDLC) ■ Frame Relay ■ Multiprotocol Label Switching (MPLS) circuit cross-connect (CCC) ■ Point-to-Point Protocol (PPP)
Cables and connectors	<ul style="list-style-type: none"> ■ Duplex LC/PC connector (RX and TX)

LEDs	<p>One tricolor per port:</p> <ul style="list-style-type: none"> ■ Off—Not enabled ■ Green—Online with no alarms or failures ■ Amber—Online with alarms for remote failures ■ Red—Active with a local alarm; router has detected a failure
Alarms, errors, and events	<ul style="list-style-type: none"> ■ Alarm Indication Signal (AIS-L, AIS-P) ■ Bit Error Rate Signal Degrade (BERR-SD), Bit Error Rate Signal Fail (BERR-SF) ■ Bit Interleaved Parity Errors B1, B2, B3 (CV-S, CV-L, CV-P) ■ Errored Seconds (ES-S, ES-L, ES-P), Far-end Bit Errors REI-L, REI-P (CV-LFE, CV-PFE), Far-end Errored Seconds (ES-LFE, ES-PFE), Far-end Severely Errored Seconds (SES-LFE, SES-PFE), Far-end Unavailable Seconds (UAS-LFE, UAS-PFE) ■ Loss of Frame (LoF), Loss of Pointer (LoP-P), Loss of Signal (LoS) ■ Payload Mismatch (PLM-P), Payload Unequipped (UNEQ-P) ■ Remote Defect Indication (RDI-L, RDI-P) ■ Severely Errored Framing (SEF), Severely Errored Framing Seconds (SEFS-S), Severely Errored Seconds (SES-S, SES-L, SES-P), Unavailable Seconds (UAS-L, UAS-P)

Table 5: Optical Interface Support for SONET/SDH OC48c/STM16 PICs

PIC Type	Single-mode Short Reach (SR)	Single-mode Long Reach (LR)
Optical interface	Single-mode short reach (Bellcore GR-253 compliant) optical interface (maximum distance 1.24 miles/2 km)	Single-mode long reach (Bellcore GR-253 compliant) optical interface (maximum distance 49.71 miles/80 km); compatible with 1550 nm single-mode LR
Wavelength	1266 through 1360 nm	1500 through 1580 nm
Average launch power	–11 through –3 dBm	–2 through +3 dBm
Receiver saturation	0 dBm	–9 dBm
Receiver sensitivity	–18 dBm	–28 dBm

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M160 Internet Router PIC Guide: End-of-Life PICs

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Cover Design: Edmonds Design

Revision History

15 January 2005—Revision 5. Added Gigabit Ethernet PICs. Updated information about installing combinations of PICs on a single Enhanced FPC.
9 November 2004—Revision 4.
17 May 2004—Revision 3.
16 March 2004—Revision 2.
24 July 2003—Revision 1.

The information in this document is current as of the date listed in the revision history.

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