Chapter 1

Interfaces Overview

This manual describes the steps you take to investigate interface problems. For each interface type, the investigation process is described in three corresponding chapters:

- Monitor the interface
- Perform a loopback test on the interface
- Locate alarms and errors

The monitor interfaces chapter helps you determine the nature of the interface problem. The loopback test chapter provides information to assist you isolate the source of the problem, and the locate alarms and errors chapter explains some of the alarms and errors for that occur on that interface.

This chapter discusses the following topics:

- Interfaces Covered in This Book on page 4
- Interfaces Supported by the JUNOS Software on page 7
- Interface Descriptors on page 9
- Interface Naming on page 11
- How Interface Configurations Are Displayed on page 15
- Interface and Router Clock Sources on page 15

Interfaces Covered in This Book

This book describes the investigation process for the following interfaces:

T1

T3

Asynchronous Transfer Mode (ATM) 1 and ATM 2 intelligent queuing (IQ)

SONET

Fast Ethernet and Gigabit Ethernet

Channelized DS-3

Multichannel DS-3

Channelized OC-12

Channelized OC-12 IQ

T1 Interfaces

T1 is the basic physical layer protocol used by the Digital Signal level 1(DS-1) multiplexing method in North America. A T1 interface operates at a bit rate of 1.544 Mbps and can support 24 DS-0 channels. The supported DS-1 standards include:

ANSI TI.107, TI.102

GR 499-core, GR 253-core

AT&T Pub 54014

ITUG.751, G.703

T3 Interfaces

T3 is the physical layer protocol used by the Digital Signal level 3 (DS-3) multiplexing method in North America. A T3 interface operates at a bit rate of 44.736 Mbps. The JUNOS software supports payload scrambling and subrate operation on each physical T3 interface. One encapsulation format—Point-to-Point Protocol (PPP), Frame Relay, or High-level Data Link Control (HDLC)—must be configured for the interface. The supported DS-3 standards include:

ANSI TI.107, TI.102

GR 499-core, GR 253-core

Bellcore TR-TSY-000009

AT&T Pub 54014

ITU G.751, G.703, G823

ATM Interfaces

ATM is a network protocol designed to facilitate the simultaneous handling of various types of traffic streams (voice, data, and video) at very high speeds over the same physical connection. By always using 53-byte cells, ATM simplifies the hardware design, enabling it to quickly determine the destination address of each cell. This allows simple switching of network traffic at much higher speeds than are easily accomplished using protocols with variable sizes of transfer units, such as Frame Relay and the Transmission Control Protocol/Internet Protocol (TCP/IP).

Although ATM was designed to operate without requiring any other networking protocol, other protocols are frequently segmented and encapsulated across multiple, smaller ATM cells, in effect making ATM a transport mechanism for preexisting technologies such as Frame Relay and the TCP/IP family of protocols.

ATM relies on the concepts of virtual paths and virtual circuits. A virtual path, represented by a specific virtual path identifier (VPI), establishes a route between two devices in a network. Each VPI can contain multiple virtual circuits, each represented by a virtual circuit identifier (VCI).

VPIs and VCIs are local to the router, which means that only the two devices connected by the VCI or VPI need to know the details of the connection. In a typical ATM network, user data might traverse multiple connections, using many different VPI and VCI connections. Each end device, just as each device in the network, needs to know only the VCI and VPI information for the path to the next device.

With the second-generation ATM2 IQ interface, you can configure virtual path shaping and operation, administration, and maintenance (OAM) F4 cell flows.

SONET Interfaces

SONET is widely used in the USA for very high-speed transmission of voice and data signals across the numerous world-wide fiber-optic networks.

SONET uses LEDs or lasers to transmit a binary stream of light-on and light-off sequences at a constant rate. At the far end, optical sensors convert the pulses of light back to electrical representations of the binary information.

In wavelength-division multiplexing (WDM), light at several different wavelengths (or colors to a human eye) is transmitted on the same fiber segment, greatly increasing the throughput of each fiber cable.

In dense wavelength-division multiplexing (DWDM), many optical data streams at different wavelengths are combined into one fiber.

The basic building block of the SONET hierarchy in the optical domain is OC-1; in the electrical domain, the basic building block is STS-1. OC-1 operates at 51.840 Mbps. OC-3 operates at 155.520 Mbps.

A SONET stream can consist of discrete lower-rate traffic flows that have been combined using Time-Division Multiplexing (TDM) techniques. This method is useful, but a portion of the total bandwidth is consumed by the TDM overhead. When a SONET stream consists of only a single, very high-speed payload, it is referred to as operating in concatenated mode. A SONET interface operating in this mode has a "c" added to the rate descriptor. For example, a concatenated OC-48 interface is referred to as OC-48c.

Fast Ethernet and Gigabit Ethernet Interfaces

Ethernet was developed in the early 1970s at the Xerox Palo Alto Research Center (PARC) as a data-link control layer protocol for interconnecting computers. It was first widely used at 10 Mbps over coaxial cables and later over unshielded twisted pairs using 10BaseT. More recently, 100BaseTX (Fast Ethernet, 100 Mbps), Gigabit Ethernet (1 Gbps), and 10-Gigabit Ethernet (10 Gbps) have become available.

Channelized Interfaces

Channelized interfaces enable you to configure a number of individual channels that subdivide the bandwidth of a larger interface and minimize the number of Physical Interface Cards (PICs) that an installation requires. Original channelized interfaces provide a single level of channelization. The newer IQ channelized PICs provide multiple levels of channelization.

Interfaces Supported by the JUNOS Software

The JUNOS software supports a greater range of interfaces than those described in this book. Future revisions of this book will include the steps for monitoring additional interfaces supported by the JUNOS software. Table 3 lists the interface types supported by the JUNOS software and shows the interface name as it appears in a configuration.

Table 3: Interface Types Supported by the JUNOS Software

Interface Name in Configuration	Interface Type	Description
ae	Aggregated Ethernet	A virtual aggregated link.
as	Aggregated SONET/SDH	A virtual aggregated link.
at	ATM1 or ATM2 IQ	Asynchronous Transfer Mode
cau4	Channelized AU-4 IQ	Configured on the Channelized STM-1 IQ PIC.
coc1	Channelized OC-1 IQ	Configured on the Channelized OC-12 IQ PIC.
coc12	Channelized OC-12 IQ	Configured on the Channelized OC-12 IQ PIC.
cstm1	Channelized STM-1 IQ	Configured on the Channelized STM-1 IQ PIC.
ce1	Channelized E1 IQ	Configured on the Channelized E1 IQ PIC or Channelized STM-1 IQ PIC.
ct1	Channelized T1 IQ	Configured on the Channelized DS-3 IQ PIC or Channelized OC-12 IQ PIC.
ct3	Channelized T3 IQ	Configured on the Channelized DS-3 IQ PIC or Channelized OC-12 IQ PIC.
cp	Collector	Configured on the Monitoring Services II PIC.
ds	DS-0	Configured on the Channelized DS-3 to DS-0 PIC, Channelized E1 PIC, Channelized OC-12 IQ PIC, Channelized DS-3 IQ PIC, Channelized E1 IQ PIC, or Channelized STM-1 IQ PIC.
dsc	Discard	Allows you to identify the ingress point of a denial-of-service (DoS) attack.
e1	E1	Includes the channelized STM-1 to E1 interfaces.
e3	E3	Includes the E3 IQ interfaces.
es	Encryption	Allows you to configure a security association (SA) name with a logical interface.
fe	Fast Ethernet	100Base-TX (Fast Ethernet, 100 Mbps).
fxp	Management and internal Ethernet	The management Ethernet interface is an out-of-band management interface within the routing platform. The internal Ethernet interface connects the Routing Engine to the Packet Forwarding Engine.
ge	Gigabit Ethernet	Includes Gigabit Ethernet IQ interfaces.
gr	Generic Route Encapsulation tunnel	Allows you to configure a unicast tunnel using GRE encapsulation.
gre	Internally generated	This interface is internally generated and is not configurable.
ip	IP-over-IP encapsulation tunnel	Allows you to configure a unicast tunnel using IP-IP encapsulation.

Interface Name in Configuration	Interface Type	Description
ipip	Internally generated	This interface is internally generated and is not configurable.
lo	Loopback	This interface is internally generated. The logical interface lo0.16383 is a non-configurable interface for routing platform control traffic.
ls	Link services	Supports bundles that contain links.
lsi	Internally generated	This interface is internally generated and is not configurable.
ml	Multilink	Includes Multilink Frame Relay and Multilink PPP.
mo	Monitoring services	Includes the monitoring services and monitoring services II interfaces. The logical interface mo-*fpc*/*pic*/*port*.16383 is an internally generated, non-configurable interface for routing platform control traffic.
mt	Multicast tunnel	Internal routing platform interface for VPNs.
mtun	Internally generated	This interface is internally generated and is not configurable.
oc3	OC-3 IQ	Configured on the Channelized OC-12 IQ PIC.
pe	This interface is present on the first-hop routing platform	Encapsulates packets destined for the rendezvous point (RP) routing platform.
pd	This interface is present on the RP	De-encapsulates packets at the RP.
pimd	Internally generated	This interface is internally generated and is not configurable.
pime	Internally generated	This interface is internally generated and is not configurable.
se	Serial	Includes the EIA-530, V.35, and X.21 interfaces.
so	SONET/SDH	Both are widely used methods for very high speed transmission of voice and data signals across the numerous world-wide fiber-optic networks.
sp	Adaptive services	The logical interface sp-*fpc*/*pic*/*port*.16383 is an internally generated, non-configurable interface for routing platform control traffic.
t1	T1	Includes the channelized DS-3 to DS-1 interfaces.
t3	T3	Includes the channelized OC-12 to DS-3 interfaces.
tap	Internally generated	This interface is internally generated and is not configurable.
vsp	Voice services	The Adaptive Services (AS) Physical Interface Card (PIC) supports the compressed real-time transport protocol (RTP) on this interface.
vt	Virtual loopback tunnel	On routing platforms equipped with a Tunnel PIC, enables egress filtering.

Interface Descriptors

When you configure an interface, you are specifying the properties for a physical interface descriptor. In most cases, the physical interface descriptor corresponds to a single physical device and consists of the following parts:

- The interface name, which defines the media type
- The slot in which the Flexible PIC Concentrator (FPC) is located
- The location on the FPC in which the PIC is installed
- The PIC port
- The channel and logical unit numbers of the interface (optional)

Each physical interface descriptor can contain one or more logical interface descriptors. These allow you to map one or more logical (or virtual) interfaces to a single physical device. Creating multiple logical interfaces is useful for ATM, Frame Relay, and Gigabit Ethernet networks, in which you can associate multiple virtual circuits, data-link connections, or virtual LANs (VLANs) with a single interface device.

Each logical interface descriptor can have one or more family descriptors to define the protocol family that it is associated with and are allowed to run over the logical interface. The following protocol families are supported:

- Internet Protocol version 4 (IPv4)
- Internet Protocol version 6 (IPv6)
- Circuit cross-connect (CCC)
- Translational cross-connect (TCC)
- International Organization for Standardization (ISO)
- Multilink Frame Relay (MLFR)
- Multilink PPP (MLPPP)
- Multiprotocol Label Switching (MPLS)
- Trivial Network Protocol (TNP)

Each family descriptor can have one or more address entries, which associate a network address with a logical interface and hence with the physical interface.

You configure the various interface descriptors as follows:

- Configure the physical interface descriptor by including the interfaces *interface-name* statement.
- Configure the logical interface descriptor by including the unit statement within the interfaces *interface-name* statement.

Configure the family descriptor by including the family statement within the unit statement.

Configure address entries by including the address statement within the family statement.

Configure tunnels by including the tunnel statement within the unit statement.

Interface Naming

Each interface has the following components:

- An interface name that specifies the media type
- The slot where the FPC is located
- The location of the PIC on the FPC
- The PIC port

The interface name uniquely identifies an individual network connector in the system. You use the interface name when configuring interfaces and when enabling various functions and properties, such as routing protocols, on individual interfaces. The system uses the interface name when displaying information about the interface, for example, in the show interfaces command.

The interface name is represented by a physical part, a logical part, and a channel part in the following format:

physical<:*channel*>.logical

The channel part of the name is optional for all interfaces except Channelized DS-3, E1, OC-12, and STM-1. For more information about channelized interfaces, see the *JUNOS Network Interfaces and Class of Service Configuration Guide*.

Physical Part of an Interface Name

The physical part of an interface name identifies the physical device, which corresponds to a single physical network connector. This part of the interface name has the following format:

type-fpc / *pic* / *port*

type is the media type, which identifies the network device. See "Interfaces Supported by the JUNOS Software" on page 7 for information on supported interface types.

fpc identifies the number of the FPC card on which the physical interface is located. Specifically, it is the number of the slot in which the FPC card is installed. M40, M40e, M160, M320, T320, and T640 platforms each have eight FPC slots that are numbered from 0 through 7 from left to right as you are facing the front of the chassis. The M20 routing platform has four FPC slots that are numbered from 0 through 3 from top to bottom as you are facing the front of the chassis. The slot number is printed adjacent to each slot. The M5, M7i, M10, and M10i routing platforms do not use FPCs; you install the PICs individually. The M5 and M7i routing platforms have space for up to four PICs. The M7i routing platform also comes with an integrated Tunnel PIC or an optional integrated AS PIC. The M10 and M10i routing platforms have space for up to eight PICs.

pic identifies the number of the PIC card on which the physical interface is located. Specifically, it is the number of the PIC location on the FPC. The four PIC slots are numbered from 0 through 3. The PIC location is printed on the FPC carrier board. For PICs that occupy more than one PIC location, use the lower location number.

port identifies a specific port on a PIC. The number of ports varies depending on the PIC. The port slot numbers are printed on the PIC.

Logical Part of an Interface Name

The logical unit part of the interface name corresponds to the logical unit number, which can be a number in the range from 0 through 16,384.

Separators in Interface Names

There is a separator of some type between each element of an interface name.

In the physical part of the name, a hyphen (-) separates the media type from the FPC number, and a slash (/) separates the FPC, PIC, and port numbers.

In the virtual part of the name, a period (.) separates the channel and logical unit numbers.

A colon (:) separates the physical and virtual parts of the interface name.

Examples: Interface Names

This section provides examples of naming interfaces. See Figure 1 for an example of where the slots, PICs, and ports are located on the M40 router. Examine your PIC to determine the port numbers; all port numbers are marked on the PIC.

Figure 1: Interface Slot, PIC, and Port Locations

For an FPC in slot 1 with two OC-3 SONET PICs in PIC positions 0 and 1, each PIC with two ports uses the following names:

```
so-1/0/0.0
so-1/0/1.0
so-1/1/0.0
so-1/1/1.0
```

An OC-48 SONET FPC in slot 1 and in concatenated mode appears as a single FPC with a single PIC, which has a single port. If this interface has a single logical unit, the name is as follows:

```
so-1/0/0.0
```

An OC-48 SONET FPC in slot 1 and in channelized mode has a number for each channel. For example:

```
so-1/0/0:0
so-1/0/0:1
```

For an FPC in slot 1 with a Channelized OC-12 PIC in PIC position 2, the DS-3 channels have the following names:

```
t3-1/2/0:0
t3-1/2/0:1
t3-1/2/0:2
...
t3-1/2/0:11
```

For an FPC in slot 1 with four OC-12 ATM PICs (the FPC is fully populated), the four PICs, each with a single port and a single logical unit, have the following names:

```
at-1/0/0.0
at-1/1/0.0
at-1/2/0.0
at-1/3/0.0
```

Channelized DS-3 to DS-0 Interface Naming

You can configure 28 T1 channels for each T3 interface. Each T1 link can have up to eight DS-0 channel groups, and each channel group can hold any combination of DS-0 time slots. To specify the T1 link and DS-0 channel group number in the interface name, use colons (:) as separators. For example, a Channelized DS-3 to DS-0 PIC might have the following physical and virtual interfaces:

ds-0/0/0:*x*:*y*

where x is a T1 link ranging from 0 through 27, and y is a DS-0 channel group ranging from 0 through 7. See the *JUNOS Internet Software Network Interfaces and Class of Service Configuration Guide* for more information about ranges.

Channelized DS-3 to DS-1 Interface Naming

You can configure 28 T1 channels per T3 interface, and each interface can have logical interfaces. To specify the channel number, include it after the colon (:) in the interface name. For example, a 4-port T3 PIC in FPC 1 and slot 1 will have the following physical interfaces, depending on the media type:

t1-1/1/0:*x*
t1-1/1/1:*x*
t1-1/1/2:*x*
t1-1/1/3:*x*

x is a channel number ranging from 0 through 27.

Channelized Intelligent Queuing Interface Naming

Channelized interfaces enable you to configure a number of individual channels that subdivide the bandwidth of a larger interface and minimize the number of PICs that an installation requires.

NOTE: Channelized IQ interfaces require M-series Enhanced FPCs.

Wherever the JUNOS documentation refers to channelized interfaces and PICs without the "intelligent queuing" or "IQ" descriptor, they are referring to the original channelized interfaces and PICs.

You can configure each port of a channelized IQ PIC as a single interface that uses the entire available bandwidth, or partition each port into smaller data channels. Following are the interface names associated with channelized IQ PICs:

coc12-*fpc*/*pic*/*port*—On a Channelized OC-12 IQ PIC

coc1-*fpc*/*pic*/*port*:*channel*—On a Channelized OC-12 IQ PIC

ct3-*fpc*/*pic*/*port*<:*channel*>—On a Channelized OC-12 IQ PIC or a Channelized DS-3 IQ PIC

cstm1-*fpc*/*pic*/*port*—On a Channelized STM-1 IQ PIC

cau4-*fpc*/*pic*/*port*:*channel*—On a Channelized STM-1 IQ PIC

ct1-*fpc*/*pic*/*port*<:*channel*>—On a Channelized OC-12 IQ PIC or a Channelized DS-3 IQ PIC

ce1-*fpc*/*pic*/*port*<:*channel*>—On a Channelized E1 IQ PIC or a Channelized STM-1 IQ PIC

e1-*fpc*/*pic*/*port*<:*channel*>—E1 channels configured on a Channelized E1 IQ or a Channelized STM-1 IQ PIC

ds-*fpc*/*pic*/*port*<:*channel*>—*Nx*DS-0 channels configured on a Channelized OC-12 IQ PIC, Channelized STM-1 IQ PIC, Channelized DS-3 IQ PIC, or Channelized E1 IQ PIC

so-*fpc*/*pic*/*port*<:*channel*>—SONET/SDH channels configure four OC-3 channels on a Channelized OC-12 IQ PIC, one OC-12 channel on a Channelized OC-12 IQ PIC, or one STM-1 channel on a Channelized STM-1 IQ PIC

t1-*fpc*/*pic*/*port*<:*channel*>—T1 channels configured on a Channelized OC-12 IQPIC or a Channelized DS-3 IQ PIC

t3-*fpc*/*pic*/*port*<:*channel*>—T3 channels configured on a Channelized OC-12 IQ PIC or a Channelized DS-3 IQ PIC

How Interface Configurations Are Displayed

When you display a configuration, using either the show command in configuration mode or the show configuration top-level command, interfaces are listed in numerical order as follows:

From lowest to highest slot number

From lowest to highest PIC number

From lowest to highest port number

Interface and Router Clock Sources

When running a loopback test on T1, T3, ATM, and SONET interfaces, you must configure the *transmit clock* . The transmit clock aligns each outgoing packet transmitted over the router's interfaces. For both the router and interfaces, the clock source can be the router's internal Stratum 3 clock, which resides on the System Control Board (SCB), the System and Switch Board (SSB), the Forwarding Engine Board (FEB), or the Miscellaneous Control Subsystem (MCS) (depending on the router model), or an external clock that is received from the interface you are configuring. For example, interface A can transmit on interface A's received clock (external, loop timing) or the Stratum 3 clock (internal, line timing). Interface A cannot use a clock from any other source.

By default, each interface uses the router's internal Stratum 3 clock. To configure the clock source of each interface, include the clocking statement at the [edit interfaces *interface-name*] hierarchy level:

```
[edit interfaces interface-name]
clocking (internal | external);
```

Figure 2 illustrates the different clock sources.

Figure 2: Clock Sources