Chapter 12

# Monitoring Key Router Components

You monitor the key router components—the Routing Engine and the Packet Forwarding Engine—to ensure that the router is handling general routing operations and is forwarding packets properly. This chapter provides an overview of the these components and includes the following information:



For information about what components comprise the Packet Forwarding Engine on each routing platform, see Table 29 on page 93.

For information about monitoring the Routing Engine, see:

# Understanding Key Router Components

**Purpose** Inspect the Routing Engine and the Packet Forwarding Engine to ensure that the router is handling general routing operations and is forwarding packets properly.

**What Are the Key Router Components**

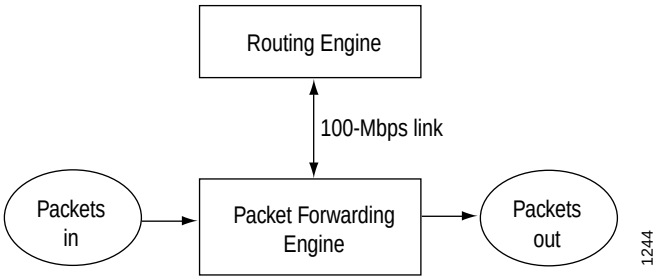
The router consists of two major architectural components:

Packet Forwarding Engine—This high-performance, application-specific integrated circuit (ASIC)-based component provides Layer 2 and Layer 3 packet switching, route lookups, and packet forwarding.

Routing Engine—Provides Layer 3 routing services and network management.

The Packet Forwarding Engine and the Routing Engine perform their primary tasks independently, although they constantly communicate through a 100-Mbps internal link. This arrangement provides streamlined forwarding and routing control and the capability to run Internet-scale backbone networks at high speeds. Figure 12 illustrates the relationship between the Packet Forwarding Engine and the Routing Engine.

**Figure 12: Router Architecture**




## *Packet Forwarding Engine*

The Packet Forwarding Engine provides Layer 2 and Layer 3 packet switching, route lookups, packet forwarding, and route lookup functions. Table 28 lists the Packet Forwarding Engine forwarding rate and aggregate throughput for each routing platform.

**Table 28: Packet Forwarding Engine Forwarding Rate and Aggregate Throughput Characteristics Per Routing Platform**

| Specifications | M5 / M10 | M7i | M10i | M20 | M40 | M40e | M160 | M320 | T320 | T640 |
|---|---|---|---|---|---|---|---|---|---|---|
| Packet forwarding rate in million packets per second (Mpps) | 40 | 16 | 16 | 40 | 40 | 40 | 160 | 385 | 385 | 770 |
| Aggregate throughput in gigabits per second (Gbps) | 6.4 | 8.4 | 12.8 | 25.6 | 40 | 51.2 | 160 | 320 | 320 | 640 |

For M-series routers, the Packet Forwarding Engine is implemented in ASICs that are located on the System Control Board (SCB): a Forwarding Engine Board (FEB) (M5/M10 router), System and Switch Board (SSB) (M20 router), SCB (M40 router), or Switching and Forwarding Module (SFM) (M40e and M160 routers). It uses a centralized route lookup engine and shared memory. For T-series routers, the Packet Forwarding Engine is implemented in ASICs that are physically located on the Flexible PIC Concentrator (FPCs) and Physical Interface Card (PICs).

Table 29 lists the Packet Forwarding Engine components for each routing platform.

**Table 29: Router Packet Forwarding Engine Components Per Routing Platform**

| Component | M5 / M10 | M7i | M10i | M20 | M40 | M40e | M160 | M320 | T320 | T640 |
|---|---|---|---|---|---|---|---|---|---|---|
| Midplane | X | X | X | X | X | X | X | X | | |
| PIC | X | X | X | X | X | X | X | X | X | X |
| FPC | Built-in | | | X | X | X | X | X | X | X |
| FIC | | X | | | | | | | | |
| CFEB | | X | X | | | | | | | |
| FEB | X | | | | | | | | | |
| SSB | | | | X | | | | | | |
| SCB | | | | | X | | | | | |
| SFM | | | | | | X | X | | | |
| Layer 2/Layer 3 Packet Processing ASIC | | | | | | | | | X | X |
| Queuing and Memory Interface ASICs | | | | | | | | X | X | X |
| T-series Internet Processor | | | | | | | | X | X | X |
| Switch Interface ASICs | | | | | | | | X | X | X |
| Media-specific ASICs on the PICs | X | X | X | X | X | X | X | X | X | X |

## Data Flow Through the Router Packet Forwarding Engine

This section describes the sequence in which data flows through each router Packet Forwarding Engine.

Data Flow Through the M5 and M10 Router Packet Forwarding Engine on page 94

Data Flow Through the M7i Router Packet Forwarding Engine on page 95

Data Flow Through the M10i Router Packet Forwarding Engine on page 96

Data Flow Through the M20 Router Packet Forwarding Engine on page 97

Data Flow Through the M40 Router Packet Forwarding Engine on page 98

Data Flow Through the M40e Router Packet Forwarding Engine on page 99

Data Flow Through the M160 Router Packet Forwarding Engine on page 100

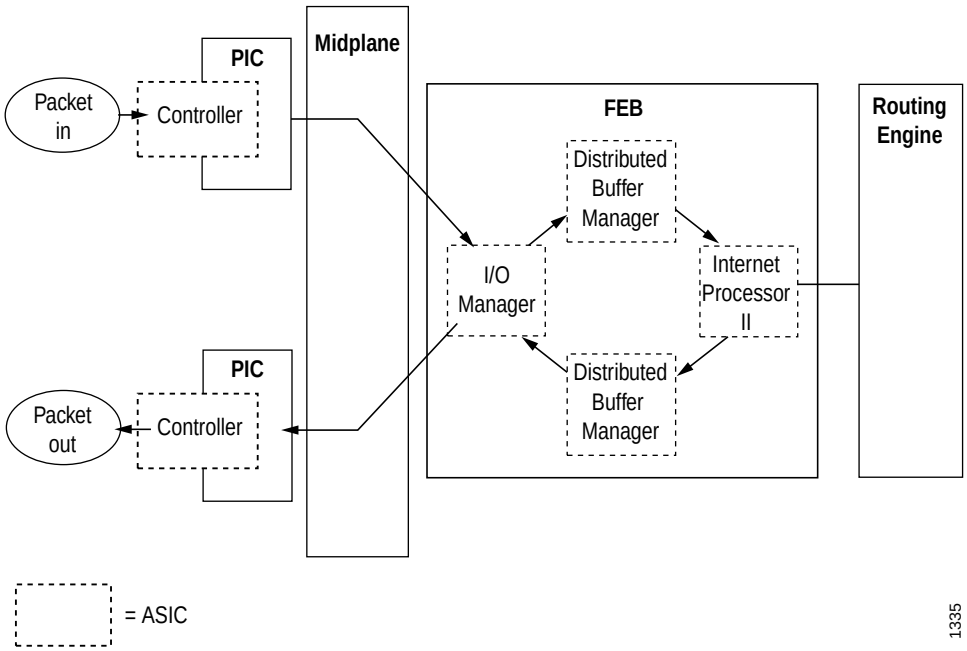
Data Flow Through the M320 Router and T640 Routing Node Packet Forwarding Engine on page 101

Data Flow Through the T320 Router and T640 Routing Node Packet Forwarding Engine on page 103

### *Data Flow Through the M5 and M10 Router Packet Forwarding Engine*

Data flows through the M5 and M10 router Packet Forwarding Engine in the sequence shown in Figure 13:

**Figure 13: M5 and M10 Router Packet Forwarding Engine Components and Data Flow**

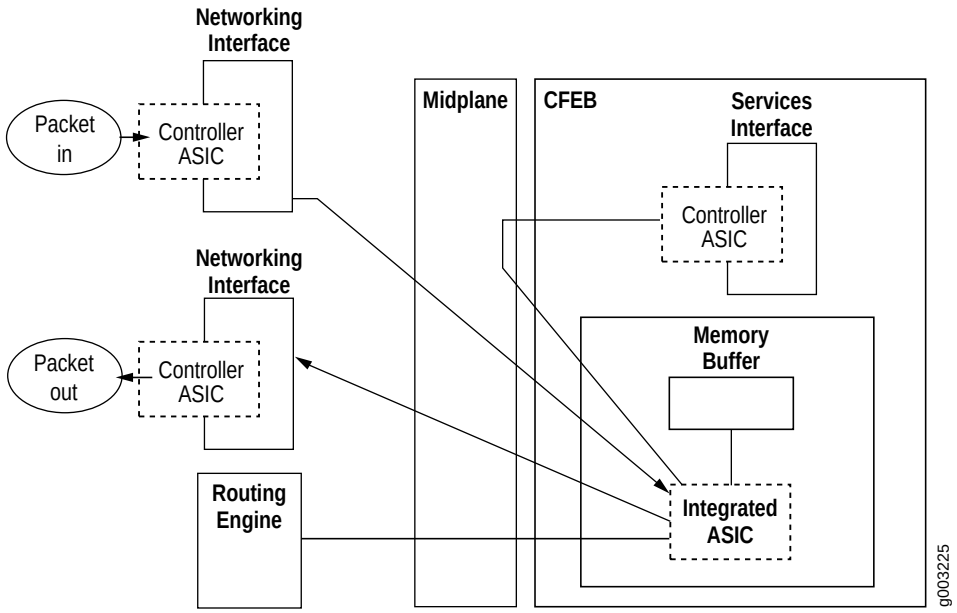



1. Packets arrive at an incoming PIC interface.
2. The PIC passes the packets through the midplane to the FEB, where the I/O Manager ASIC breaks them into 64-byte cells.
3. The Distributed Buffer Manager ASIC on the FEB distributes the data cells throughout memory banks on the FEB.
4. The Internet Processor II ASIC on the FEB performs route lookups and makes forwarding decisions.
5. The Internet Processor II ASIC notifies a second Distributed Buffer Manager ASIC on the FEB, which forwards the notification to the outgoing interface.
6. The I/O Manager ASIC on the FEB reassembles data cells in shared memory into data packets as they are ready for transmission and passes them to the outgoing PIC through the midplane.
7. The outgoing PIC transmits the data packets.

### *Data Flow Through the M7i Router Packet Forwarding Engine*

Data flows through the M7i router Packet Forwarding Engine in the following sequence shown in Figure 14. Use of ASICs promotes efficient movement of data packets through the system.

**Figure 14: M7i Router Packet Forwarding Engine Components and Data Flow**




1. Packets arrive at an incoming networking interface.

2. The networking interface passes the packets to the CFEB, where the integrated ASIC processes the packet headers, divides the packets into 64-byte data cells, and distributes the data cells throughout the memory buffer.

3. The integrated ASIC on the CFEB performs a route lookup for each packet and decides how to forward it.

    a. If services are configured for the packet, the integrated ASIC reassembles the packet and passes it to the services interface.

    b. The services interface passes the packet to the CFEB, where the integrated ASIC processes the packet, divides the packet into 64-byte cells, and distributes the data cells throughout the memory buffer.

    c. The integrated ASIC performs a second route lookup for each packet and decides how to forward it.

4. The integrated ASIC notifies the outbound networking interface.

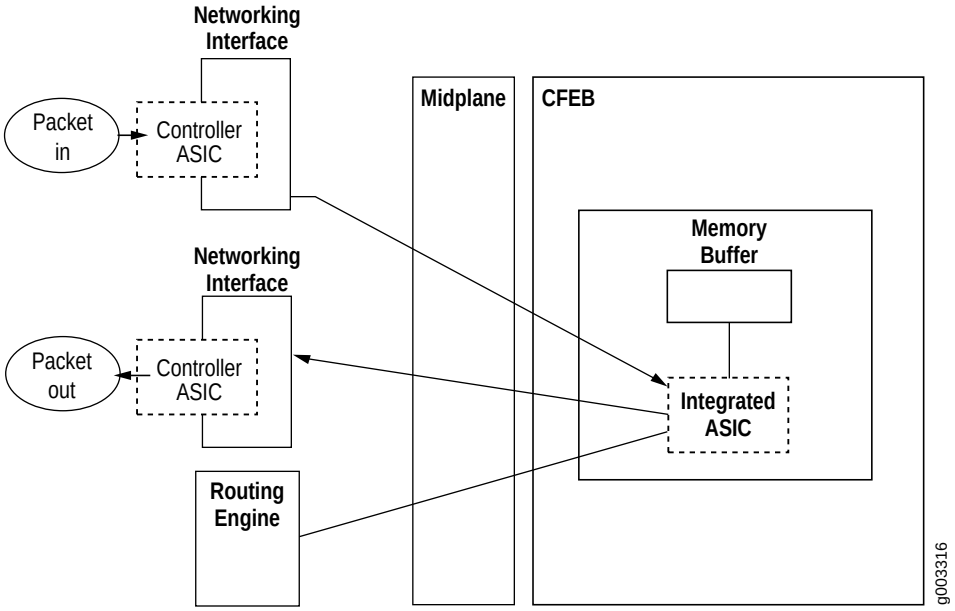
5. The integrated ASIC reassembles data cells stored in shared memory into data packets as they are ready for transmission and passes them to the outbound networking interface.

6. The outbound networking interface transmits the data packets.

### *Data Flow Through the M10i Router Packet Forwarding Engine*

Data flows through the M10i routers Packet Forwarding Engine in the sequence shown in Figure 15. Use of ASICs promotes efficient movement of data packets through the system.

**Figure 15: M10i Router Packet Forwarding Engine Components and Data Flow**

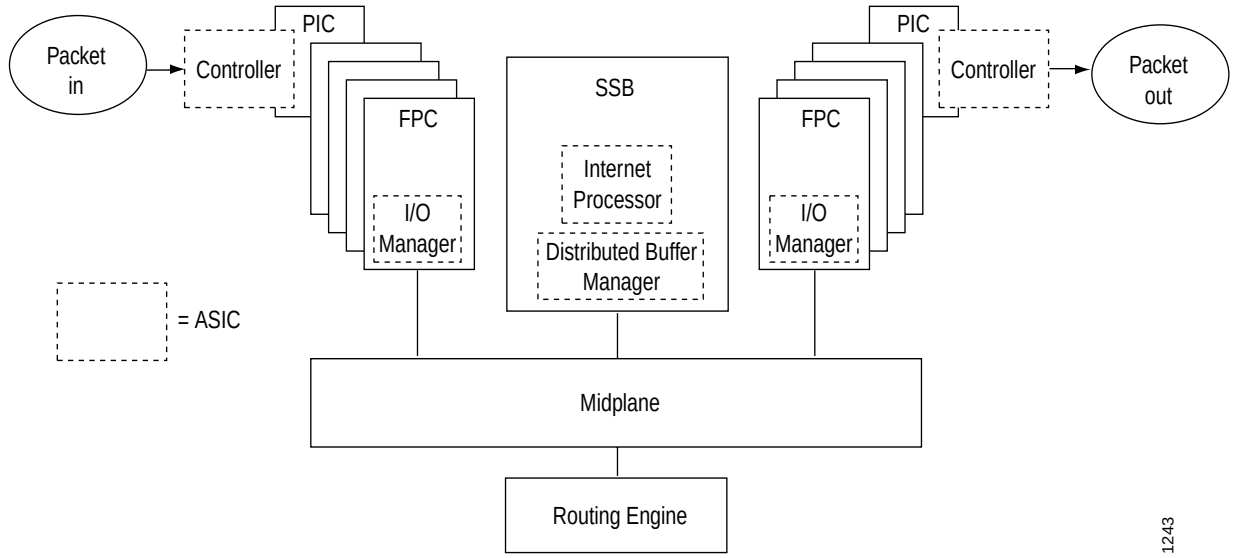



1. Packets arrive at an incoming networking interface.
2. The networking interface passes the packets to the CFEB, where the integrated ASIC processes the packet headers, divides the packets into 64-byte data cells, and distributes the data cells throughout the memory buffer.
3. The integrated ASIC on the CFEB performs a route lookup for each packet and decides how to forward it.
    a. If services are configured for the packet, the integrated ASIC reassembles the packet and passes it to the services interface.
    b. The services interface passes the packet to the CFEB, where the integrated ASIC processes the packet, divides the packet into 64-byte cells, and distributes the data cells throughout the memory buffer.
    c. The integrated ASIC performs a second route lookup for each packet and decides how to forward it.
4. The integrated ASIC notifies the outbound networking interface.
5. The integrated ASIC reassembles data cells stored in shared memory into data packets as they are ready for transmission and passes them to the outbound networking interface.
6. The outbound networking interface transmits the data packets.

### *Data Flow Through the M20 Router Packet Forwarding Engine*

Data flows through the M20 router Packet Forwarding Engine in the sequence shown in Figure 16.

**Figure 16: M20 Router Packet Forwarding Engine Components and Data Flow**

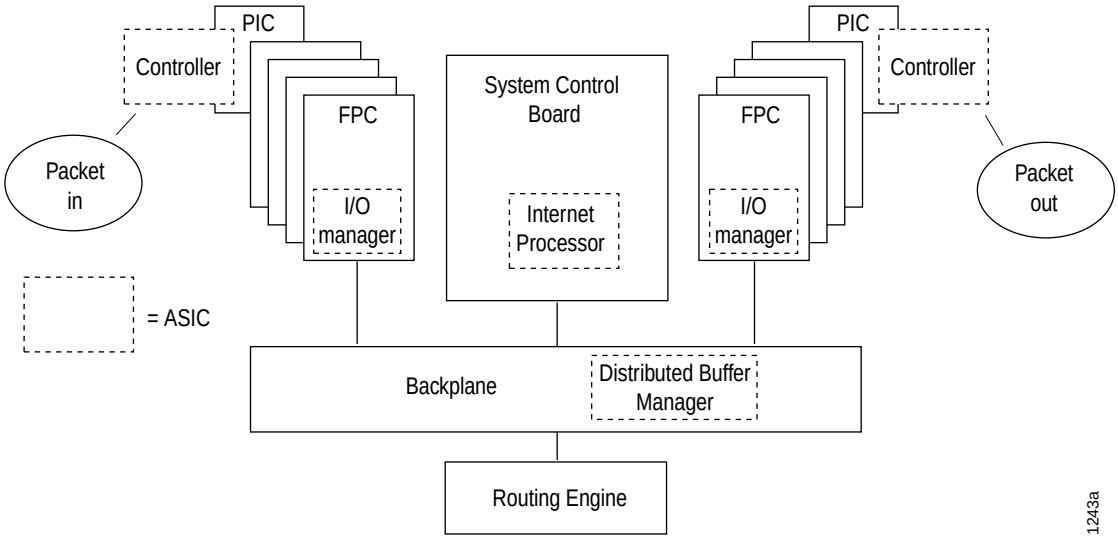



1. Packets arrive at an incoming PIC interface.
2. The I/O Manager ASIC processes the packet headers, divides the packets into 64-byte data cells, and passes the cells through the midplane to the SSB.
3. A Distributed Buffer Manager ASIC on the SSB distributes the data cells throughout the memory buffers located on and shared by all the FPCs.
4. The Internet Processor II ASIC on the SSB performs a route lookup for each packet and decides how to forward it.
5. The Internet Processor II ASIC notifies a Distributed Buffer Manager ASIC on the SSB of the forwarding decision, and the Distributed Buffer Manager ASIC forwards the notification to the FPC that hosts the appropriate outbound interface.
6. The I/O Manager ASIC on the FPC reassembles data cells stored in shared memory into data packets as they are ready for transmission and passes them through the Packet Director ASIC to the outbound PIC.
7. The outbound PIC transmits the data packets.

### *Data Flow Through the M40 Router Packet Forwarding Engine*

Data flows through the M40 router Packet Forwarding Engine in the sequence shown in Figure 17.

**Figure 17: M40 Router Packet Forwarding Engine Components and Data Flow**

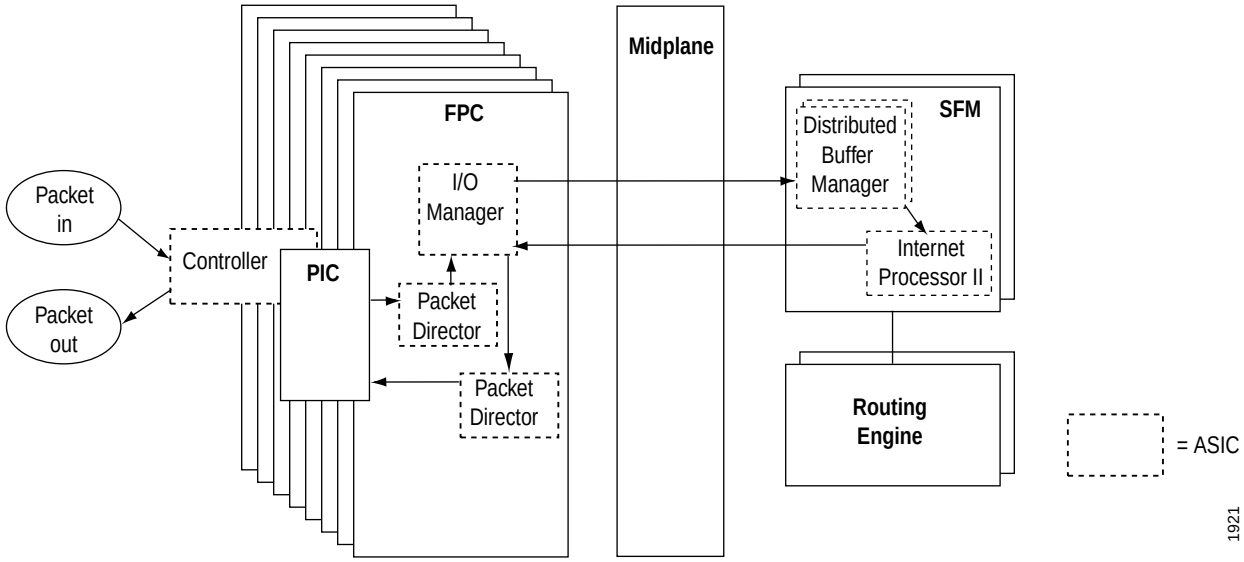



1. Packets arrive at an incoming PIC interface.
2. The PIC passes the packets to the FPC, where the I/O Manager ASIC processes the packet headers, divides the packets into 64-byte data cells, and passes the cells to the backplane.
3. The Distributed Buffer Manager ASIC on the backplane distributes the data cells throughout the memory buffers located on and shared by all the FPCs.
4. The Internet Processor or Internet Processor II ASIC on the SCB performs route lookups and makes forwarding decisions.
5. The Internet Processor or Internet Processor II ASIC notifies a second Distributed Buffer Manager ASIC on the backplane of the routing decision.
6. The Distributed Buffer Manager ASIC forwards the notification to the FPC that hosts the outbound PIC.
7. The I/O Manager ASIC on the FPC reassembles data cells in shared memory into data packets as they are ready for transmission and passes them to the outbound PIC.
8. The outbound PIC transmits the data packets.

### *Data Flow Through the M40e Router Packet Forwarding Engine*

Data flows through the M40e router Packet Forwarding Engine in the sequence shown Figure 18.

**Figure 18: M40e Router Packet Forwarding Engine Components and Data Flow**

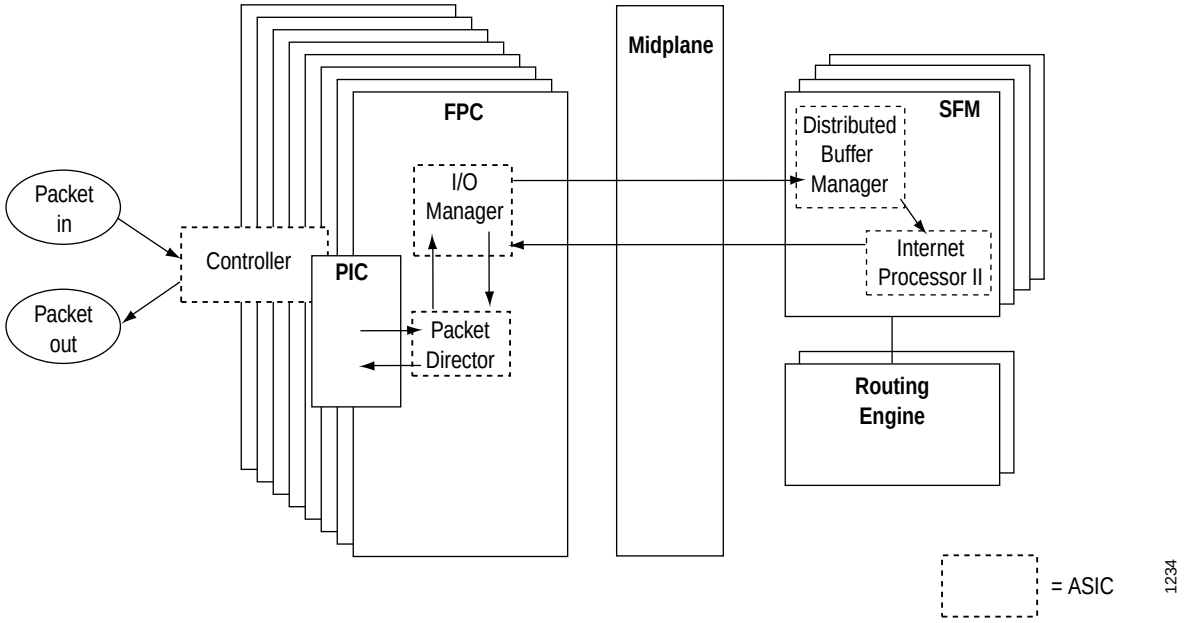



1. Packets arrive at an incoming PIC interface.
2. The PIC passes the packets to the FPC, where the Packet Director ASIC directs them to the active I/O Manager ASIC.
3. The I/O Manager ASIC processes the packet headers, divides the packets into 64-byte data cells, and passes the cells through the midplane to the SFM.
4. A Distributed Buffer Manager ASIC on the SFM distributes the data cells throughout the memory buffers located on and shared by all the FPCs.
5. The Internet Processor II ASIC on the SFM performs a route lookup for each packet and decides how to forward it.
6. The Internet Processor II ASIC notifies the second Distributed Buffer Manager ASIC (on the SFM) of the forwarding decision, and the Distributed Buffer Manager ASIC forwards the notification to the FPC that hosts the appropriate outbound interface.
7. The I/O Manager ASIC on the FPC reassembles data cells stored in shared memory into data packets as they are ready for transmission and passes them through the Packet Director ASIC to the outbound PIC.
8. The outbound PIC transmits the data packets.

### *Data Flow Through the M160 Router Packet Forwarding Engine*

Data flows through the M160 router Packet Forwarding Engine in the sequence shown in Figure 19.

**Figure 19: M160 Router Packet Forwarding Engine Components and Data Flow**

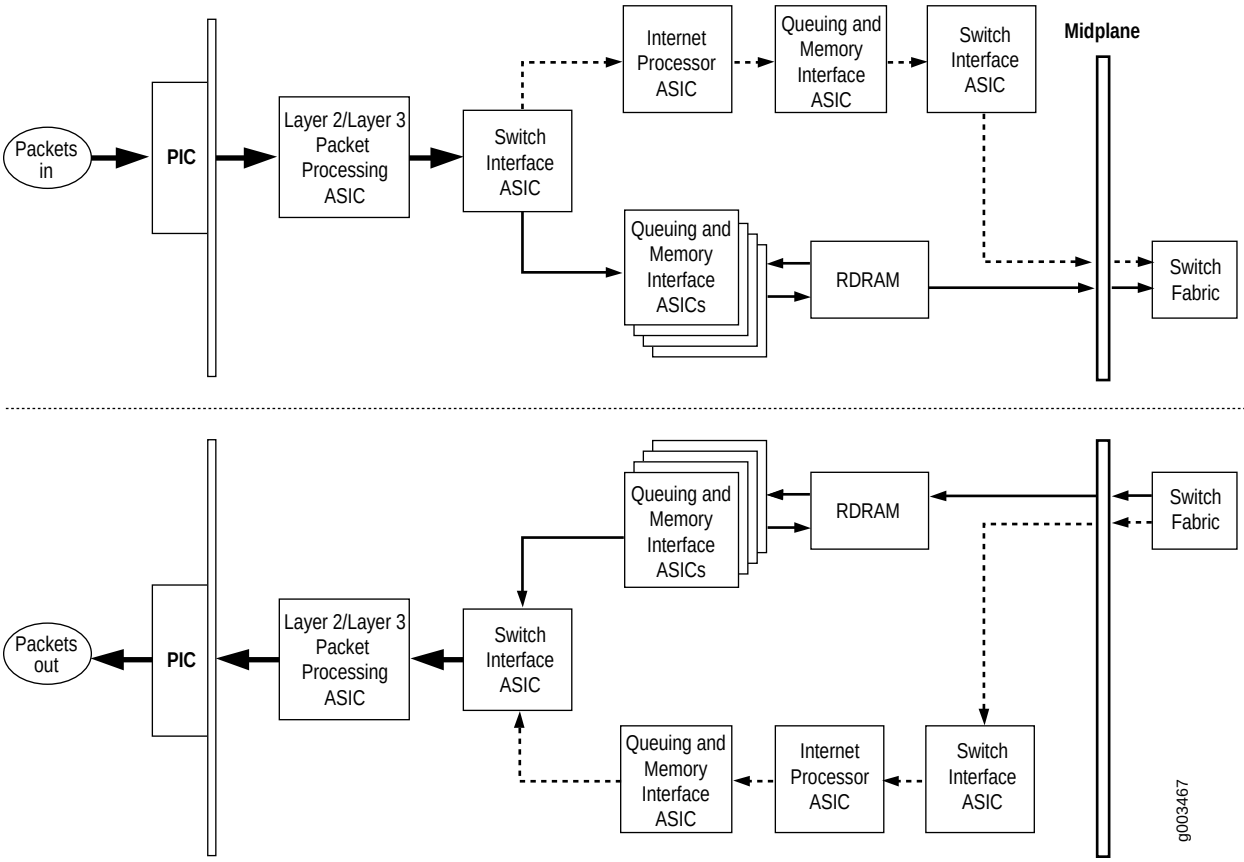



1. Packets arrive at an incoming PIC interface.
2. The PIC passes the packets to the FPC, where the Packet Director ASIC distributes them among the I/O Manager ASICs.
3. The I/O Manager ASICs process the packet headers, divide the packets into 64-byte data cells, and pass the cells through the midplane to the SFMs.
4. The Distributed Buffer Manager ASICs on the SFMs distribute the data cells throughout memory buffers located on and shared by all the FPCs.
5. For each packet, an Internet Processor II ASIC on an SFM performs a route lookup and decides how to forward the packet.
6. The Internet Processor II ASIC notifies a second Distributed Buffer Manager ASIC (on the SFM) of the forwarding decision, and the Distributed Buffer Manager ASIC forwards the notification to the FPC that hosts the appropriate outbound interface.
7. The I/O Manager ASIC on the FPC reassembles data cells in shared memory into data packets as they are ready for transmission and passes them through the Packet Director ASIC to the outbound PIC.
8. The outbound PIC transmits the data packets.

### *Data Flow Through the M320 Router and T640 Routing Node Packet Forwarding Engine*

Data flows through the M320 routing node Packet Forwarding Engine in the sequence shown Figure 20.

**Figure 20: M320 Router Packet Forwarding Engine Components and Data Flow**




1. Packets arrive at an incoming PIC interface.

2. The PIC passes the packets to the FPC, where the Layer 2/Layer 3 Packet Processing ASIC performs Layer 2 and Layer 3 parsing and divides the packets into 64-byte cells.

3. The Switch Interface ASIC extracts the route lookup key, places it in a notification and passes the notification to the Internet Processor ASIC. The Switch Interface ASIC also passes the data cells to the Queuing and Memory Interface ASICs for buffering.

4. The Queuing and Memory Interface ASICs pass the data cells to memory for buffering.

5. The Internet Processor ASIC performs the route lookup and forwards the notification to the Queuing and Memory Interface ASIC.

6. The Queuing and Memory Interface ASIC sends the notification to the Switch Interface ASIC facing the switch fabric, unless the destination is on the same Packet Forwarding Engine. In this case, the notification is sent back to the Switch Interface ASIC facing the outgoing ports, and the packets are sent to the outgoing port without passing through the switch fabric (see Step 13).

7. The Switch Interface ASIC sends bandwidth requests through the switch fabric to the destination port. The Switch Interface ASIC also issues read requests to the Queuing and Memory Interface ASIC to begin reading data cells out of memory.

8. The destination Switch Interface ASIC sends bandwidth grants through the switch fabric to the originating Switch Interface ASIC.

9. Upon receipt of each bandwidth grant, the originating Switch Interface ASIC sends a cell through the switch fabric to the destination Packet Forwarding Engine.

10. The destination Switch Interface ASIC receives cells from the switch fabric. It extracts the route lookup key from each cell, places it in a notification, and forwards the notification to the Internet Processor ASIC.

11. The Internet Processor ASIC performs the route lookup, and forwards the notification to the Queuing and Memory Interface ASIC.

12. The Queuing and Memory Interface ASIC forwards the notification, including next-hop information, to the Switch Interface ASIC.

13. The Switch Interface ASIC sends read requests to the Queuing and Memory Interface ASIC to read the data cells out of memory, and passes the cells to the Layer 2/Layer 3 Packet Processing ASIC.

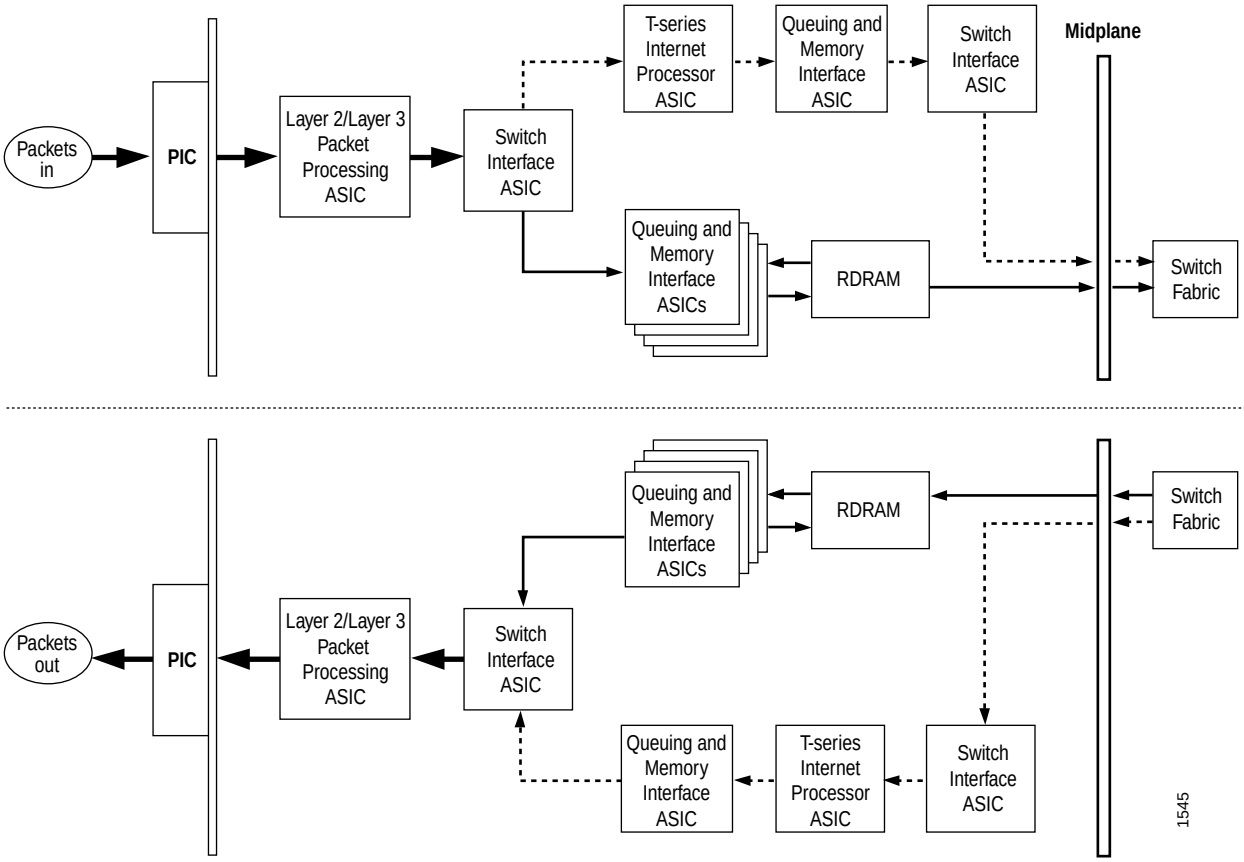
14. The Layer 2/Layer 3 Packet Processing ASIC reassembles the data cells into packets, adds Layer 2 encapsulation, and sends the packets to the outgoing PIC interface.

15. The outgoing PIC sends the packets out into the network.

### *Data Flow Through the T320 Router and T640 Routing Node Packet Forwarding Engine*

Data flows through the T320 router and T640 routing node Packet Forwarding Engine in the following sequence shown in Figure 21.

**Figure 21: T320 Router and T640 Routing Node Packet Forwarding Engine Components and Data Flow**




1. Packets arrive at an incoming PIC interface.

2. The PIC passes the packets to the FPC, where the Layer 2/Layer 3 Packet Processing ASIC performs Layer 2 and Layer 3 parsing and divides the packets into 64-byte cells.

3. The Switch Interface ASIC extracts the route lookup key, places it in a notification, and passes the notification to the T-series Internet Processor. The Switch Interface ASIC also passes the data cells to the Queuing and Memory Interface ASICs for buffering.

4. The Queuing and Memory Interface ASICs pass the data cells to memory for buffering.

5. The T-series Internet Processor performs the route lookup and forwards the notification to the Queuing and Memory Interface ASIC.

6. The Queuing and Memory Interface ASIC sends the notification to the Switch Interface ASIC facing the switch fabric, unless the destination is on the same Packet Forwarding Engine. In this case, the notification is sent back to the Switch Interface ASIC facing the outgoing ports, and the packets are sent to the outgoing port without passing through the switch fabric (see Step 13).

7. The Switch Interface ASIC sends bandwidth requests through the switch fabric to the destination port. The Switch Interface ASIC also issues read requests to the Queuing and Memory Interface ASIC to begin reading data cells out of memory.

8. The destination Switch Interface ASIC sends bandwidth grants through the switch fabric to the originating Switch Interface ASIC.

9. Upon receipt of each bandwidth grant, the originating Switch Interface ASIC sends a cell through the switch fabric to the destination Packet Forwarding Engine.

10. The destination Switch Interface ASIC receives cells from the switch fabric. It extracts the route lookup key from each cell, places it in a notification, and forwards the notification to the T-series Internet Processor.

11. The T-series Internet Processor performs the route lookup, and forwards the notification to the Queuing and Memory Interface ASIC.

12. The Queuing and Memory Interface ASIC forwards the notification, including next-hop information, to the Switch Interface ASIC.

13. The Switch Interface ASIC sends read requests to the Queuing and Memory Interface ASIC to read the data cells out of memory, and passes the cells to the Layer 2/Layer 3 Packet Processing ASIC.

14. The Layer 2/Layer 3 Packet Processing ASIC reassembles the data cells into packets, adds Layer 2 encapsulation, and sends the packets to the outgoing PIC interface.

15. The outgoing PIC sends the packets out into the network.

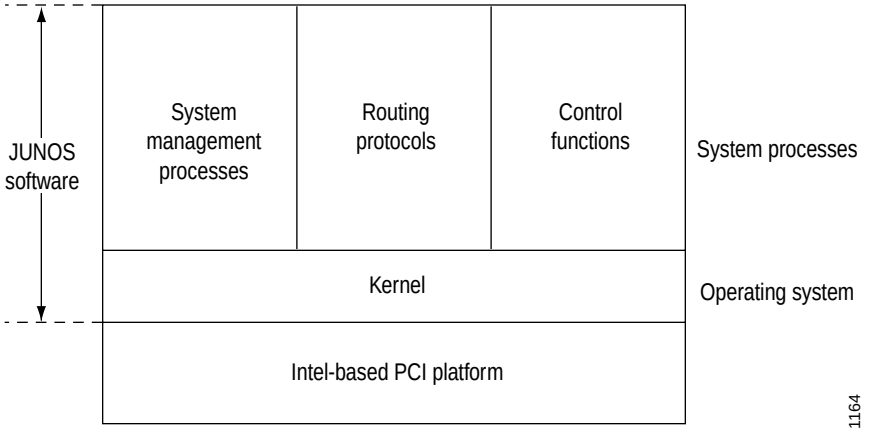
## Routing Engine

The Routing Engine consists of JUNOS software running on an Intel-based Peripheral Component Interconnect (PCI) platform. The JUNOS kernel supports JUNOS system processes which handle system management processes, routing protocols, and control functions (see Figure 22 on page 105).

The Routing Engine handles all the routing protocol processes, as well as other software processes that control the router interfaces, the chassis components, system management, and user access to the router. These routing and software processes run on top of a kernel that interacts with the Packet Forwarding Engine.

The Routing Engine has a dedicated 100-Mbps internal connection to the Packet Forwarding Engine.

**Figure 22: Routing Engine Architecture**




## Routing Engine Functions

The Routing Engine handles all the routing protocol processes, as well as other software processes that control the router interfaces, system management, and user access to the router. These routing and software processes run on top of a kernel that interacts with the T-series Internet Processor in the Packet Forwarding Engine.

The Routing Engine provides the following functions:

Routing protocol packet processing—All routing protocol packets from the network are directed to the Routing Engine, and hence do not delay the Packet Forwarding Engine unnecessarily.

Software modularity—By dividing the different software functions into separate processes, the failure of one process is isolated from others and has little or no effect on them.

In-depth Internet functionality—Each routing protocol is implemented with a complete set of Internet features and provides full flexibility for advertising, filtering, and modifying routes. Routing policies are set according to route parameters (such as prefix, prefix lengths, and BGP attributes).

Scalability—The JUNOS routing tables are designed to hold all the routes in current and imminent networks. Additionally, the JUNOS software efficiently supports large numbers of interfaces and virtual circuits.

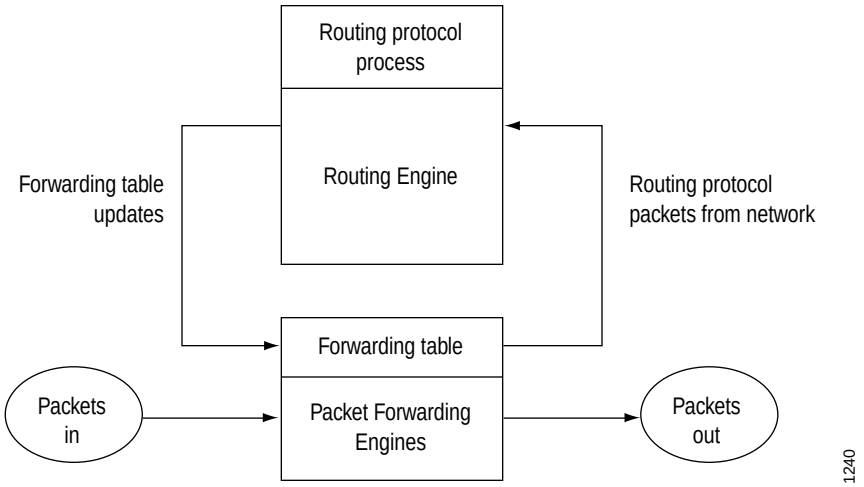
Management interface—Different levels of system management practices are provided, including a command-line interface (CLI) and SNMP.

Storage and change management—Configuration files, system images, and microcode can be held and maintained in primary and secondary storage systems, permitting local or remote upgrades.

Efficiency and flexibility monitoring—The router permits alarm handling and packet counting. For example, the router allows information to be gathered on every port, without adversely affecting packet forwarding performance.

The Routing Engine constructs and maintains one or more routing tables (see Figure 23). From the routing tables, the Routing Engine derives a table of active routes, called the *forwarding table*, which is copied into the Packet Forwarding Engines. The design of the T-series Internet Processor allows the forwarding table in the Packet Forwarding Engines to be updated without interrupting the router's forwarding.

**Figure 23: Control Packet Handling for Routing and Forwarding Table Update**




On the M320 and T320 routers and the T640 routing node, the host subsystem provides the routing and system management functions. The host subsystem consists of the Routing Engine and the Control Board. For more information about the host subsystem, see "Monitoring the Host Subsystem" on page 289. For more information about the Control Boards, see "Monitoring the Control Board" on page 301.

On the M40e and M160 routers, the host module provides the routing and system management functions. The host module consists of the Routing Engine and the Miscellaneous Control Subsystem (MCS). For more information about the host module, see "Monitoring the Host Module" on page 341. For more information about the MCS, see "Monitoring the MCS" on page 359.

On the M10i router, the Routing Engine works with its companion High-Availability Chassis Manager (HCM) to provide control and monitoring functions for router components. For more information about the HCM, see "Monitoring the HCM" on page 431.