Configuring the Channelized T3 Loop Timing

By default, internal clocking (line timing) is used on channelized IQ and IQE interfaces. To configure SONET/SDH or DS3-level external clocking, include the loop-timing statement:

```
loop-timing;
```

You can include this statement at the following hierarchy levels:

- [edit interfaces ct3-*fpc/pic/port* t3-options]
- [edit interfaces stm1-*fpc/pic/port* sonet-options]

To explicitly configure the default line timing, include the no-loop-timing statement in the configuration:

```
no-loop-timing;
```

The loop-timing and no-loop-timing statements apply only to E1 and T1 interfaces you configure on channelized IQ and IQE PICs. If you attempt to include these statements on any other interface type, they are ignored.

For all channelized IQ and IQE PICs, the clocking statement is supported on all channels. To configure clocking on individual interfaces, include the clocking statement at the [edit interfaces *type-fpc/pic/port*:*channel*] hierarchy level. If you do not include the clocking statement, the individual interfaces use internal clocking by default.

For more information, see Configuring the Clock Source and [Unresolved xref].