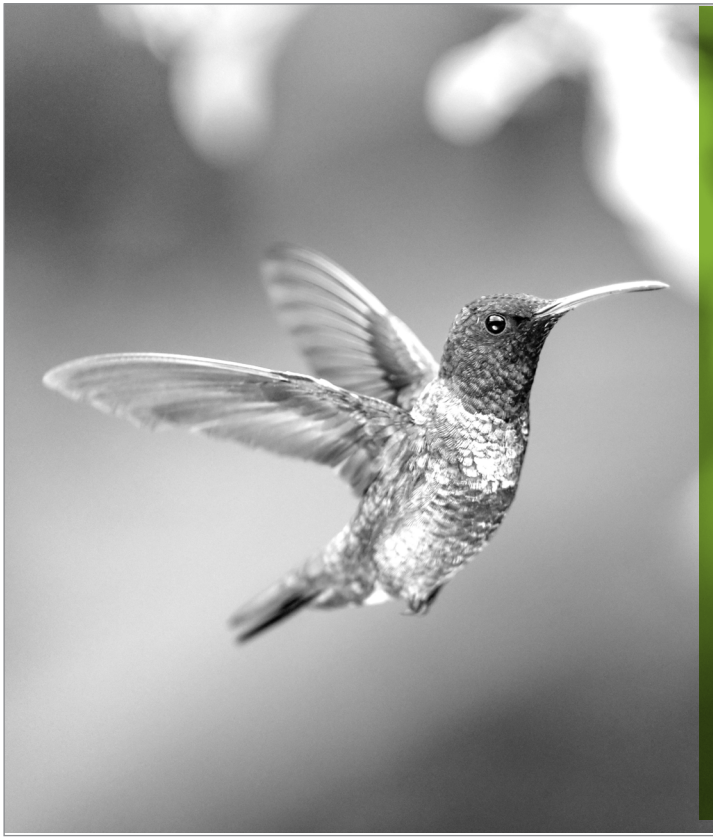
JUNIPER NETWORKS | Engineering Simplicity

DAY ONE: DEPLOYING JUNOS® TIMING AND SYNCHRONIZATION



Synchronization requirements are becoming more stringent and widely spread with the advent of 5G technologies and services such as High Accuracy Positioning as well as applications like Autonomous Vehicles that require precise synchronization. Learn more about the critical applications and Junos timing solutions using PTP and SyncE.

By Satheesh Kumar S

DAY ONE: DEPLOYING JUNOS® TIMING AND SYNCHRONIZATION

Day One: Deploying Junos® Timing and Synchronization provides a detailed overview of timing and synchronization with an insight on the underlying technologies and how Junos (and Junos EVO) can help the reader with the configurations for various deployments. From clocks to packets to network design, this book is a complete journey into the synchronization issues of modern networks, and uniquely, how to configure, debug, and troubleshoot most of them. It's all here with compact descriptions, configuration samples, and a hundred illustrations.

"Definitely, a must have book into the nuances of timing and synchronous Ethernet. It can help anyone gain basic knowledge of PTP and SyncE to seamlessly deploy Timing solutions"

Prashanth A S, Software Engineering Sr Director, Juniper Networks

"Timing is an all-important function for 5G rollout and Satheesh takes the reader from basics to configuration and troubleshooting SyncE and PTP using various network topology use cases. It's a must-read book for everyone who needs to understand Junos timing functionality and how it works across Juniper product lines."

Vijay Kulkarni, Software Engineering Director, Juniper Networks

"Timing and synchronization have stringent requirements for 5G networks, the transport networks, and mobile carriers. This book is coming out at an opportune time and Satheesh covers the entire gamut, from the basics of synchronization, to the various deployment models and support on Juniper devices, to listing all the various standards and specifications. This is a valuable addition to the Day One library."

Sharath Kaggundi, Software Engineer Staff, Juniper Networks

IT'S DAY ONE AND YOU HAVE A JOB TO DO, SO LEARN ABOUT:

- The various applications of synchronization and their requirements.
- Synchronous Ethernet technology and how to work with various configuration options and failover scenarios.
- How PTP works with various profile configurations and advantage of one profile over other.
- Clock advertisement across the network and how the network handles failover scenarios.
- Design and deploying the devices in various use cases.
- Configuring, verifying, debugging, and troubleshooting basic issues.
- Packet decodes of various PTP packets, which will enable deeper analysis of the various options and attributes that are used in PTP communications.

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Juniper Networks Books are focused on network reliability and efficiency.

Peruse the complete library at www.juniper.net/dayone..

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NOTE While publishing this book, the IEEE1588v2 standard bodies had not yet converged on a *Master/Slave* terminology alternative. So this book uses *Master/Client* instead of Master/Slave in descriptive text and figures, but leaves "slave" in CLI code and output. As soon as the standards bodies agree, the book will be updated.

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About the Author

Satheesh Kumar S is a Software Engineer Sr Staff with Juniper Networks, Bangalore, India. He has over 18 years of experience across multiple domains L1/L2/L3 technologies, Timing and Synchronization and MEF features. He is MEF3.0-CECP-D certified. He has published a few IEEE papers in the international conferences in the area of Timing and Synchronization and has authored/co-authored 3 US patents. He has extensive experience in the solution validation, design, analyse, and debug in the Synchronization area. In his spare time, he tries to read and understand on emerging technologies and also enjoys spending time with his family. He holds a Master of Technology in Optical Communications. Aside from Juniper Networks, he worked at Ericsson and Ciena corporation. This *Day One* book is an attempt to share the Timing and Synchronization expertise with readers.

Author's Acknowledgement

Writing this *Day One* book on Timing and Synchronization to me, is just consolidating the knowledge I have learned from various experts in this area over many years. A very special thank you to Kamatchi Gopalakrishnan from Juniper Networks for helping all these years with his humungous knowledge in the Timing and Synchronization technology.

I would like to thank my parents, my wife, Nisha, and my two daughters, Mrinal and Mithila, for all their encouragement and support. A great thank you to Prashant Naik, Rafik P and Sharath Kaggundi for their technical review, and many thanks to Editor in Chief Patrick Ames and our copyeditor, Nancy Koerbel, for their timely assistance and guidance with the book.

I am also grateful to my manager Vijay Kulkarni for supporting and encouraging to write this book. Thanks to Prashant A S, Vijay Kulkarni and Sharath Kaggundi for their quotes on the book. Last but not least, thanks to all my colleagues who in many ways helped me to contribute to this book. Satheesh Kumar S, Software Engineer Sr Staff, MEF-CECP-D.

What You Need to Know Before Reading This Book

- You need a basic understanding of Junos (or Junos EVO) CLI and configurations. See the *Day One* books at www.juniper.net/books for a variety of books at all skill levels.
- You need a basic understanding of Synchronization. You should be conversant with handling various clocking test equipment and tools, a familiarity with Paragon-x, at least, is must.
- You need a basic understanding of Synchronous Ethernet and Precision Time Protocol.
- This book assumes that you have a basic understanding of networking and will be able to configure and troubleshoot IP Addressing and basic switching and routing configurations.
- You will need access to two or three Juniper Networks devices that support synchronization features and be able to install a Junos (or Junos EVO) Software version that supports Timing and Synchronization features that are discussed in this book.
- You will need access to a Timing Test tool with a proper reference clock that enables clocking to signal to the device under test. Hands-on learning will be possible even without access to the test device.

By Reading This Book ...

- You will be familiar with various applications of synchronization and their requirements.
- You will learn Synchronous Ethernet technology and will learn to work with various configuration options and fail-over scenarios.
- You will learn the PTP clock synchronization and state machine. You will learn how PTP works with supported profile configurations and the advantage of one profile over the other.
- You will learn PTP clock advertisement across the network and how the network handle fail-over scenarios.
- You will learn how to deploy the devices in various use cases.
- You will learn configuring, verifying, debugging and troubleshooting basic issues.
- You will learn the clock specifications and network limits and the applicable performance measurements.
- You will get an overview of various ITU-T recommendations.
- You will learn the packet decodes of various PTP packets, which will enable deeper analysis of the various options and attributes that are used in PTP communications.

How This Book Is Set Up

This book is organized in seven chapters and an Appendix. The first chapter gives the reader a general introduction to clock synchronization and its requirements in various applications. It gives the user a summary of various Juniper platforms supporting synchronization.

Chapters 2 and 3 delve into physical layer synchronization and various concepts of PTP and profiles. Configurations on various PTP and SyncE features are illustrated with linear, ring, and other network topologies and verification of these features in normal and failover scenarios. Basic trouble shooting practices on PTP and SyncE are also discussed.

Chapter 4 gives an overview of TC and its configuration and verifications.

In Chapter 5, the reader is taken through various deployment scenarios and configurations.

Chapter 6 delves into the performance metrics of clock specifications and network limits as per ITU-T, and Chapter 7 gives an overview of ITU-T recommendations for Frequency and Phase.

Chapter 7 is followed by an Appendix that documents the Packet decodes.

Timing Resources in the Juniper TechLibrary

The list of available timing resources in the Juniper TechLibrary is excellent and thorough, and it is constantly updated. Be sure to familiarize yourself with this valuable information.

Synchronous Ethernet Overview	https://www.juniper.net/documentation/en_US/junos/topics/concept/ethernet-synchronous-overview.html
Ethernet Synchronization Message Channel Overview	https://www.juniper.net/documentation/en_US/junos/topics/concept/ethernet-synchronization-message-channel-overview.html
Synchronous Ethernet on 10-Gigabit Ethernet MIC Overview	https://www.juniper.net/documentation/en_US/junos/topics/concept/ethernet-synchronous-10ge-xfp-overview.html
Understanding ESMC Quality Level Mapping	https://www.juniper.net/documentation/en_US/junos/topics/concept/ethernet-esmc-clock-class-mapping-overview.html
Configuring Synchronous Ethernet on MX Series Routers	https://www.juniper.net/documentation/en_US/junos/topics/example/example-configuring-synchronous-ethernet.html
Configuring Framing Mode for Synchronous Ethernet on MX Series Routers with 10-Gigabit Ethernet MIC	https://www.juniper.net/documentation/en_US/junos/topics/example/synchronous-ethernet-on-mx-with-10-ge-interfaces.html
Centralized Clocking Overview	https://www.juniper.net/documentation/en_US/junos/topics/concept/chassis_centralized_clocking_overview.html
Understanding Clock Synchronization	https://www.juniper.net/documentation/en_US/junos/topics/concept/chassis-external-clock-synchronization-interface-understanding-mx.html
Getting Started Configuring Clock Synchronization on PTX Series Routers	https://www.juniper.net/documentation/en_US/junos/topics/concept/clock-synchronization-ptx-get-started.html
Interface and Router Clock Sources Overview	https://www.juniper.net/documentation/en_US/junos/topics/concept/interfaces-interface-and-router-clock-sources-overview.html
Configuring External Clock Synchronization Interface for M Series, MX Series, and T Series Routers	https://www.juniper.net/documentation/en_US/junos/topics/task/configuration/chassis-external-clock-synchronization-interface-configuring.html
Configuring Clock Synchronization Interface on MX Series Routers	https://www.juniper.net/documentation/en_US/junos/topics/task/configuration/chassis-external-clock-synchronization-interface-configuring-mx.html
Clock Sources for PTX Series Packet Transport Routers	https://www.juniper.net/documentation/en_US/junos/topics/concept/ptx-router-clock-sources.html

Synchronizing Internal Stratum 3 Clock to External Clock Sources on PTX Series Routers	https://www.juniper.net/documentation/en_US/junos/topics/task/configuration/chassis-external-clock-synchronization-ptx.html
Configuring Centralized Clocking on the Enhanced MX Switch Control Board	https://www.juniper.net/documentation/en_US/junos/topics/example/centralized-clocking-scbe-mx-configuring.html
Configuring Centralized Clocking on an MX2020	https://www.juniper.net/documentation/en_US/junos/topics/example/centralized-clocking-mx2020-configuring.html
Understanding Hybrid Mode	https://www.juniper.net/documentation/en_US/junos/topics/concept/hybrid-mode-overview.html
Configuring Hybrid Mode and ESMC Quality Level Mapping	https://www.juniper.net/documentation/en_US/junos/topics/task/configuration/ethernet-hybrid-mode-configuring.html
Configuring Hybrid Mode and ESMC Quality Level Mapping-Example	https://www.juniper.net/documentation/en_US/junos/topics/example/ethernet-hybrid-mode-configuring.html
Precision Time Protocol Overview	https://www.juniper.net/documentation/en_US/junos/topics/concept/ptp-overview.html
Configuring G.8275.1 Profile	https://www.juniper.net/documentation/en_US/junos/topics/task/configuration/ptp-telecom-profile-configuring.html
Line Card Redundancy Overview	https://www.juniper.net/documentation/en_US/junos/topics/concept/line-card-redundancy-overview.html
Configuring Precision Time Protocol	https://www.juniper.net/documentation/en_US/junos/topics/task/configuration/ethernet-ptp-configuring.html
Configuring Precision Time Protocol-Example	https://www.juniper.net/documentation/en_US/junos/topics/example/ethernet-ptp-configuring.html
Understanding Transparent Clocks in Precision Time Protocol	https://www.juniper.net/documentation/en_US/junos/topics/concept/ptp-transparent-clock-overview.html
IEEE 1588v2 PTP Boundary Clock Overview	https://www.juniper.net/documentation/en_US/junos/topics/concept/ptp-boundary-clock-overview.html
IEEE 1588v2 Precision Timing Protocol (PTP)	https://www.juniper.net/documentation/en_US/junos/topics/concept/ptp-overview-acx-series.html

Understanding the PTP G.8275.2 Enhanced Profile (Telecom Profile)	https://www.juniper.net/documentation/en_US/junos/topics/concept/ptp-telecom-profile-overview-qfx-series.html
Understanding the PTP Media Profiles	https://www.juniper.net/documentation/en_US/junos/topics/concept/ptp-media-profile-overview-qfx-series.html
PTP over Ethernet on ACX Series Routers Overview	https://www.juniper.net/documentation/en_US/junos/topics/concept/ptp-over-ethernet-overview-acx-series.html
Guidelines for Configuring PTP over Ethernet	https://www.juniper.net/documentation/en_US/junos/topics/concept/ptp-over-ethernet-configuration-guidelines.html
Understanding the Precision Time Protocol Enterprise Profile	https://www.juniper.net/documentation/en_US/junos/topics/concept/ptp-enterprise-profile-overview-qfx-series.html
Configuring Transparent Clock Mode for Precision Time Protocol	https://www.juniper.net/documentation/en_US/junos/topics/task/configuration/ptp-transparent-clock.html
Configuring a PTP Transparent Clock	https://www.juniper.net/documentation/en_US/junos/topics/task/configuration/ptp-transparent-clock-acx500.html
Configuring the Precision Time Protocol G.8275.2 Enhanced Profile (Telecom Profile)	https://www.juniper.net/documentation/en_US/junos/topics/task/configuration/telecom-profile-configuring-qfx-series.html
Configuring the PTP Media Profiles	https://www.juniper.net/documentation/en_US/junos/topics/task/configuration/ptp-media-profile-configuring-qfx-series.html
Configuring Precision Time Protocol Default Profile	https://www.juniper.net/documentation/en_US/junos/topics/task/configuration/ethernet-ptp-configuring-qfx-series.html
Configuring the Precision Time Protocol Enterprise Profile	https://www.juniper.net/documentation/en_US/junos/topics/task/configuration/enterprise-profile-configuring-qfx-series.html
Configuring Precision Time Protocol Clocking	https://www.juniper.net/documentation/en_US/junos/topics/task/configuration/ptp-parameters.html
Configuring a PTP Master Boundary Clock	https://www.juniper.net/documentation/en_US/junos/topics/task/configuration/ptp-master-clock.html
Configuring a PTP Boundary Clock	https://www.juniper.net/documentation/en_US/junos/topics/example/ptp-boundary-clock-without-unicast-negotiation.html

Configuring a PTP Boundary Clock With Unicast Negotiation	https://www.juniper.net/documentation/en_US/junos/topics/example/ptp-boundary-clock-with-unicast-negotiation.html
Configuring a PTP Slave Clock	https://www.juniper.net/documentation/en_US/junos/topics/task/configuration/ptp-slave-clock.html
Configuring an Ordinary Slave Clock With Unicast-Negotiation	https://www.juniper.net/documentation/en_US/junos/topics/example/slave-clock-with-unicast-negotiation-acx-series.html
Configuring an Ordinary Slave Clock Without Unicast-Negotiation	https://www.juniper.net/documentation/en_US/junos/topics/example/slave-clock-no-unicast-negotiation-acx-series.html
Configuring Precision Time Protocol Over Integrated Routing and Bridging	https://www.juniper.net/documentation/en_US/junos/topics/task/configuration/ptp-over-irb-acx.html
Configuring PHY Timestamping	https://www.juniper.net/documentation/en_US/junos/topics/task/configuration/phy-timestamping-acx.html
Configuring PHY Timestamping on ACX2200 Routers	https://www.juniper.net/documentation/en_US/junos/topics/task/configuration/phy-timestamping-acx2200.html
G.703 2.048MHz Signal Type for BITS Interfaces Overview	https://www.juniper.net/documentation/en_US/junos/topics/concept/bits-interfaces-g-703-signal-type.html
Configuring PTP Multicast Master and Slave Ports for Ethernet Encapsulation	https://www.juniper.net/documentation/en_US/junos/topics/task/configuration/ptp-over-ethernet-multicast-master-slave-ports.html
Configuring PTP Dynamic Ports for Ethernet Encapsulation	https://www.juniper.net/documentation/en_US/junos/topics/task/configuration/ptp-over-ethernet-dynamic-ports.html
Configuring PTP over Ethernet for Multicast Master, Slave, and Dynamic Ports	https://www.juniper.net/documentation/en_US/junos/topics/example/ptp-over-ethernet-multicast-master-slave-dynamic-ports-configuration.html
Hybrid Mode on ACX Series Routers Overview	https://www.juniper.net/documentation/en_US/junos/topics/concept/hybrid-mode-overview-acx-series.html

Guidelines for Configuring Hybrid Mode on ACX Series Routers	https://www.juniper.net/documentation/en_US/junos/topics/concept/hybrid-mode-guidelines-acx-series.html
Configuring Hybrid Mode and ESMC Quality Level Mapping on ACX Series Routers	https://www.juniper.net/documentation/en_US/junos/topics/task/configuration/ethernet-hybrid-mode-configuring-acx-series.html
Configuring Hybrid Mode and ESMC Quality Level Mapping	https://www.juniper.net/documentation/en_US/junos/topics/example/ethernet-hybrid-mode-configuring-acx-series.html
Understanding Timing Defects and Event Management on ACX Series	https://www.juniper.net/documentation/en_US/junos/topics/concept/understanding-defects-event-management-for-timing-acx500-series.html
Understanding SNMP MIB for Timing on ACX Series	https://www.juniper.net/documentation/en_US/junos/topics/concept/understanding-snmp-timing-acx-series.html

Chapter 1

Introduction to Synchronization

Time is so ubiquitous that everyone in this world can understand the importance of time keeping. Synchronization is related to timekeeping. Time synchronization plays a pivotal role in almost every walk of modern communications, especially in mobile backhaul applications. And now, with the advent of 5G, synchronization requirements are much more stringent and more widely spread.

The mobile communication industry is one of the biggest drivers behind network timekeeping and synchronization. Mobile technology requires that base stations not only synchronize in frequency but also in time. This helps the base stations to cooperate with each other in a timely manner in order to share available resources and also to increase capacity. There are a number of ways to enable Frequency and Time synchronization for base stations, and though GPS is one of the more widely used solutions, a packet method of synchronization transfer is the one most preferred in next generation networks considering the scalability and feasibility in the synchronization deployment. The industry today is capable of providing timing accuracy of 10s of ns or better on a single node with packet-based synchronization method.

Although the title of this book is *Deploying Junos Timing and Synchronization*, it is certainly not an attempt to provide a complete insight into every timing and synchronization option on every single platform sold by Juniper Networks. It aims to provide the reader with an overview of timing and synchronization with an insight into the underlying technology and how the Junos operating system (and Junos EVO) helps the reader implement the configurations for various deployments.

NOTE This book replaces the terms “master” and “slave” clocks with the terms “master” and “client” clocks.

Clock Definitions

An ideal clock is periodic in nature with sharp rising and trailing edges as shown in Figure 1.1. You can see that this clock is extending from $-\infty\ to\ +\infty$. Let's discuss some of important parameters of a clock.

Figure 1.1 Ideal Clock

Frequency

Frequency is a measure of the occurrence of significant edges of the clock. The frequency associated with this clock is:

$$f = \left(\frac{1}{T}\right) Hz$$

$'T'$ is the Time period of the clock. This is the time interval between the two significant instants of the clock. Frequency is also used to represent offset. In this case it is expressed in parts-per-million (ppm).

Phase

Phase is the value of time at significant edges of the clock. Two clocks are said to be phase aligned, if their significant edges align with an acceptable tolerance. The rate of change of Phase gives the Frequency.

Time

Time usually represents the Time of Day (TOD). It is defined as "the duration of 9,192,631,770 periods of the radiation corresponding to the transition between two hyperfine levels of the ground state of the cesium-133 atom". Two clocks are said to be time aligned, if the time of day occurrences of the significant edges align with an acceptable tolerance.

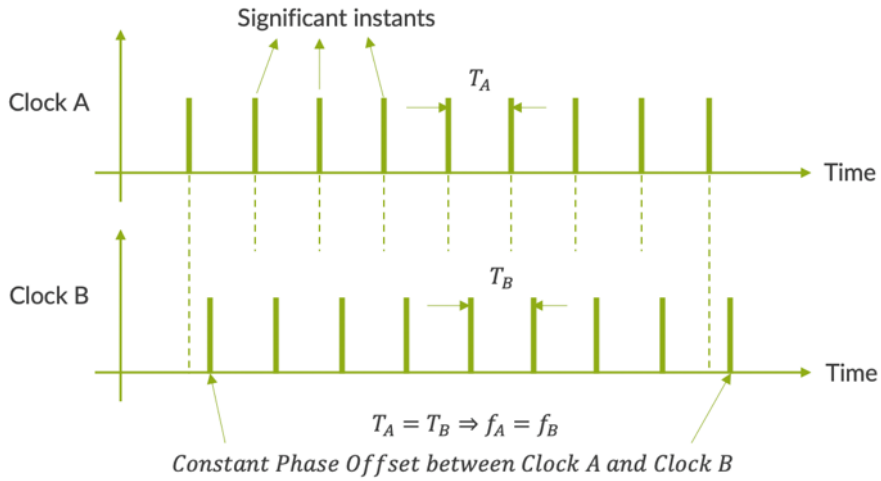
Jitter and Wander

Both Jitter and Wander are termed as manifestations of clock phase-noise. Jitter is defined as short-term variations in time of the significant instances of a clock with respect to a reference clock. Noise beyond 10Hz is considered as Jitter whereas, that below 10Hz is referred as Wander. Both Jitter and Wan-der are usually expressed in unit intervals (UI). One UI is one time period of the clock signal. For example, for a 10MHz clock signal, one UI is 100 ns. So, a jitter/wander accumulation of $1\mu sec$, can be expressed as 10 UI.

Frequency, Phase, and Time Synchronization

Let's begin with frequency synchronization and with Figure 1.2's illustration of the frequency synchronization between two clocks, A and B.

Figure 1.2 Frequency Synchronization



An ideal clock is usually represented as a square wave. The rising edges of the square wave are taken as a reference point in time. These edges are called "*significant instants*" in ITU-T parlance. If the significant instants of the clocks A and B occur with same frequency or periodicity by maintaining either constant or zero phase offset between the two, then they are said to be *frequency synchronized*. In clocks that are frequency synchronized,

$$T_A = T_B$$

$$f_A = f_B$$

Phase Offset between clock A and clock B=0 or Constant.

Now let's understand Phase Synchronization.

Figure 1.3 Phase Synchronization

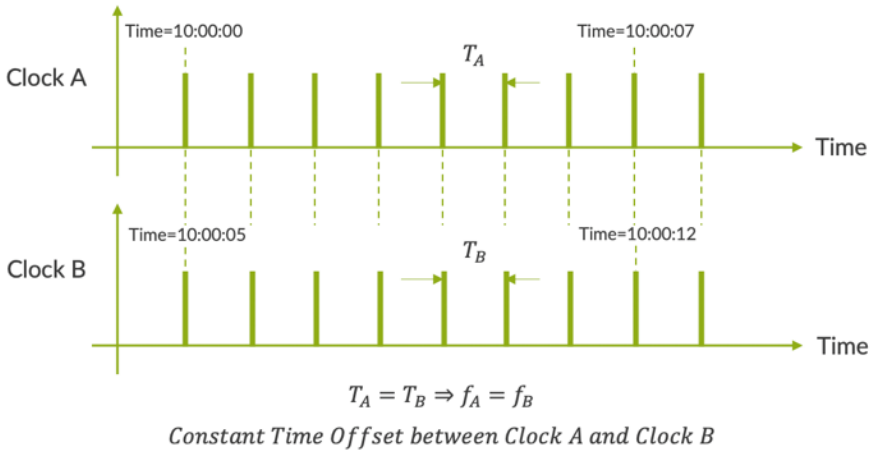


Figure 1.3 depicts the phase synchronization between two clocks, A and B. The two clocks are said to be *phase synchronized* if the significant instants occur not only at the same rate but also at the same time. So, two clocks are phase synchronized if,

$$T_A = T_B$$

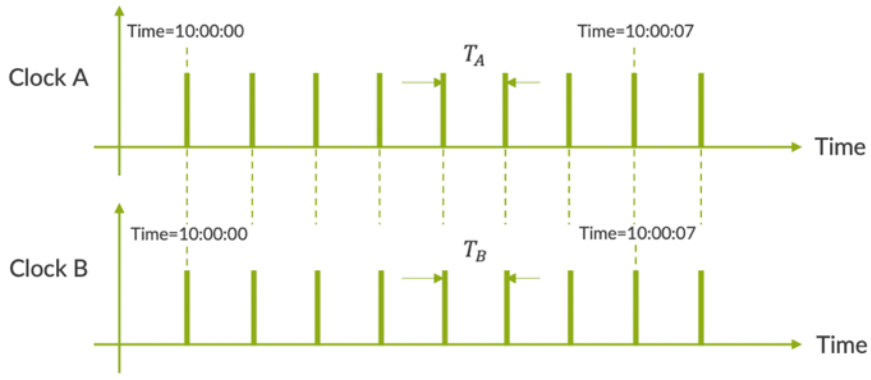
$$f_A = f_B$$

$$Phase\ Offset\ between\ clock\ A\ and\ clock\ B = 0$$

$$Time\ Offset\ between\ clock\ A\ and\ clock\ B = 0\ or\ Constant$$

It is apparent that the two clocks that are phase synchronized are also frequency synchronized. However, they need not be time synchronized.

Figure 1.4 Time Synchronization



Time Synchronization between two clocks, A and B, is illustrated in the Figure 1.4. You can see that when the two clocks are time synchronized, the time offset between two clocks at any given significant instant is zero. Time synchronization implies phase synchronization, therefore significant instants happen at the same time. It also implies that the two nodes are frequency synchronized. So, two nodes are time synchronized if,

$$T_A = T_B$$

$$f_A = f_B$$

$$Phase\ Offset\ between\ clock\ A\ and\ clock\ B = 0$$

$$Time\ Offset\ between\ clock\ A\ and\ clock\ B = 0$$

Most of the Time Division Duplex systems require Time Synchronization, examples of which are Mobile WiMAX, WCDMA TDD, and LTE TDD.

Clock Metrics

To better understand the quality of clocks and network synchronization, it is important to know some of the most important parameters that are frequently used in synchronization. Let's discuss these in this section.

Frequency Error or Accuracy

Frequency Accuracy is a measure of how accurate the clock under measurement is with respect to the ideal standard reference clock. For all practical measurements a stable Primary Reference Clock (PRC) or a Primary Reference Source (PRS) traceable to stratum1 clock is used as the reference clock. This could be 2 Mbps, 2 MHz or 10 MHz viz.

It is recommended to use a high frequency clock as the reference with more frequent rising & trailing edges.

$$F_m \; is \; the \; measured \; frequency \; of \; the \; clock$$

$$F_r \; is \; the \; frequency \; of \; the \; reference \; clock$$

Then the frequency error is

$$\Delta f = (F_m - F_r)Hz$$

A more useful and practical parameter is Fractional Frequency offset (FFO).

$$Fractional \; Frequency \; Offset \; (FFO) = \frac{\Delta f}{F_r} = \frac{(F_m - F_r)}{F_r}$$

The frequency requirement of a mobile network at the air interface is 16 PPB, which translates to a backhaul requirement of approximately 50 PPB (~3x 16 PPB), which means the allowed tolerance of

$$\pm 45Hz \; error \; at \; 900 \; MHz \; of \; Carrier \; Frequency$$

Frequency accuracy plays a critical role in cellular networks typically during handoff the signal from one base station to another. We will discuss this in detail in the subsequent section.

Phase Error or Phase Noise

Phase Error is a phase deviation of the significant instants of two clocks observed at certain instant of time. These clocks may have their origin at different time in the past. This means that these two clocks are expected to have a constant initial offset. Phase noise of a clock describes the instability of the frequency of the clock expressed in the frequency domain.

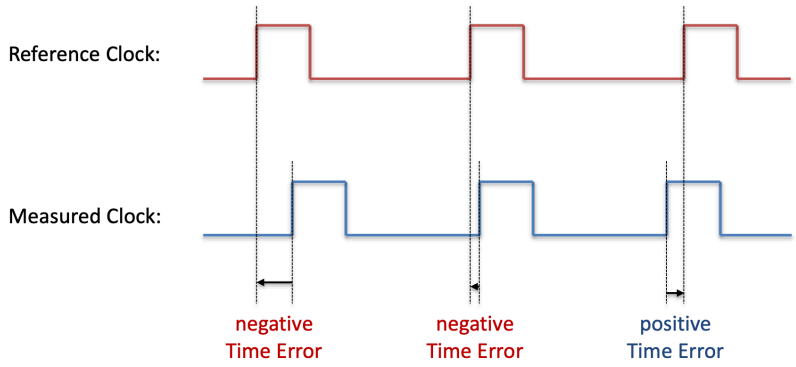
Frequency Stability

It is a measure of the intrinsic stability of the clock. It refers to the ability of an oscillator to maintain its frequency even though it may be subject to varying environmental conditions. It is a measure of the frequency change averaged over observation interval. This is computed through standard deviation of phase error predictions and the metric is usually expressed by the term TDEV.

Time Error

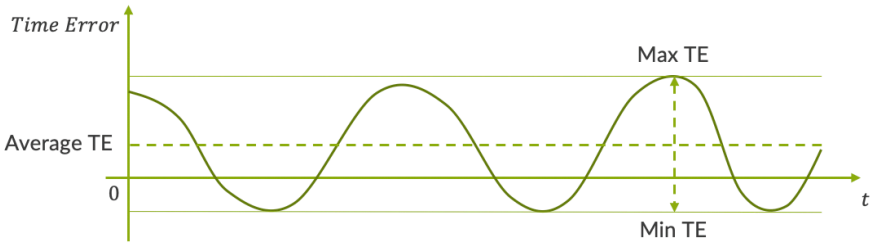
To understand the meaning of Time Error (TE), let us illustrate with a scenario shown in Figure 1.5.

Figure 1.5 Time Error-Illustration



We all know that clock is specified by the edges, typically rising edges of a train of pulses. Let us consider two clocks, clock1 and clock2. The clock 1 is the ideal reference clock with time base of UTC and clock 2 is the measurement clock whose parameters are to be analyzed with respect to that of clock 1. We assume both of these clocks had no error and their origin started at some instant of time say, $t = t_0$. We can see that at a later time, the significant edges of the clock2 lagging behind the reference clock by a small amount. The error is **negative** in this case. However, a little later, where the significant edge happened to be advances from that of the reference. The error is **positive** in this case. This deviation of the significant edges of the clock with respect to the reference is called Time Error at that instant, which is truly a manifestation of the clock noise. Figure 1.6 below plots TE vs observation time.

Figure 1.6 Time Error Plot



The peak-to-peak value of the time error is usually known as the Dynamic time error (dTE) and the average value of the time error is known as constant time error (cTE). Typically, the averaging period is 1000 seconds.

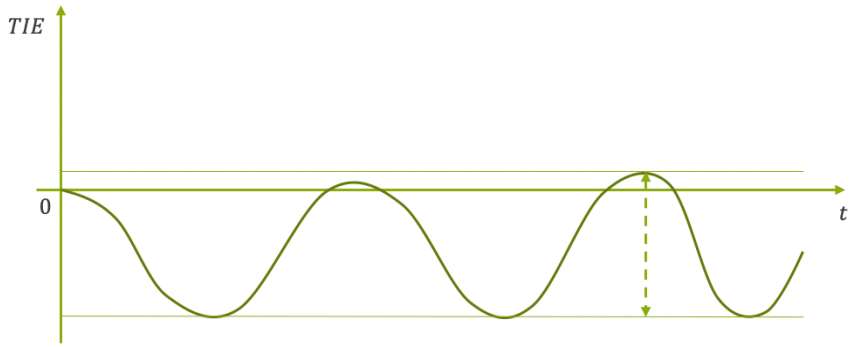
$$x(t) = cTE + dTE,$$

$$'dTE' \text{ is the signed variation around the mean value}$$

Time Interval Error

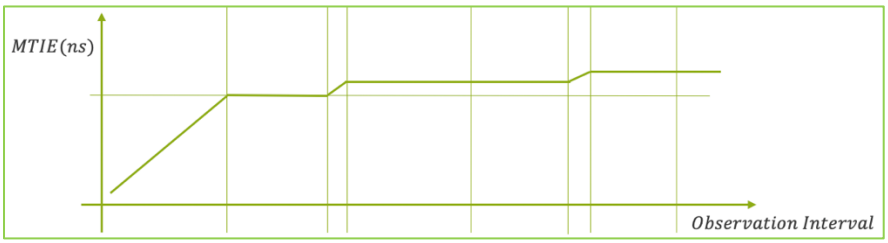
Time Interval Error (TIE) is the difference in time error (TE) of the clock over a specified interval. It is more of a relative term unlike time error. Figure 1.7 below plots the TIE vs Time Interval. One can easily understand that the Time Interval Error is nothing but the normalized Time Error to the 1st data point. The max peak-to-peak value represents the Maximum TIE ($MTIE$) for the entire observation interval.

Figure 1.7 Time Interval Error Plot



In fact $MTIE$ is calculated by a sliding window algorithm using different observation interval and calculate the largest phase wander in the given observation interval. The plot of such $MTIE$ against time always show either increasing or constant $MTIE$ as the observation window size increases. Linear increase in $MTIE$ indicate a constant frequency offset. For smaller value of observation interval τ, the $MTIE(\tau)$ is mainly due to Jitter. For medium τ, $MTIE(\tau)$ is due to wander and for large τ, indicates that the device is locked. The Figure 1.8 below gives the plot of $MTIE$.

Figure 1.8 MTIE Plot



Why Do We Need Synchronization?

Many services and applications that run on modern networks require accurate synchronization for their correct operation. Before we jump into various synchronization technologies and how they work in Junos (and Junos EVO), it is important to understand the various services and applications that impose stringent requirements on synchronization. More precisely, let's try to answer the question: *Why do we need synchronization?*

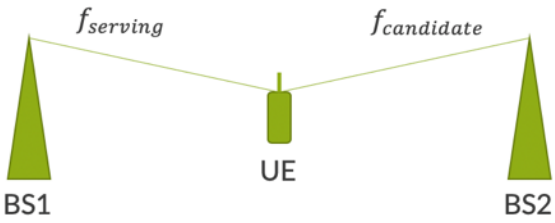
Synchronization plays a vital role in digital communication networks where data is sent as a series of bits, which are either 0s or 1s. The data is usually encoded as a series of clock pulses at the transmitter side. The value of 1 is typically represented by non-zero positive voltage, and bit 0 is represented by 0 voltage. The transition between 0s and 1s are represented by the edge of the pulse, typically rising edge.

At the receiving side, the data is recovered using these edges of the clock pulse. For efficient clock recovery, you need to have more edges, and therefore, to have enough transitions in the data transmitted, different *line coding* was invented. With line coding, it may not be always true that 1 is always represented by positive value and 0 by 0 voltage, but for the transfer of data from transmitter to receiver, the bit period on both sides needs to align properly, else the receiver would end up reading inaccurate data. In other words, for faithful data transmission, the Tx clock on the transmitter and Rx clock on the receiver should be same.

Figure 1.9 Synchronization-Data Communication Network

Another important application of synchronization is in the field of mobile technologies. Frequency synchronization is always required in mobile networks to allow handover of the User Equipment (UE) between the base stations. When UE moves from the serving base station to the candidate base station, it should lock in frequency to the candidate base station with an acceptable tolerance to avoid interference and crosstalk (see Figure 1.10). This imposes a maximum tolerance to the frequency generated by the base station (BS) over the radio interface, typically 50 parts per billion (ppb) of frequency error. Another reason synchronization places constraints on the maximum frequency deviation of a BS is to comply with regulatory aspects generating a signal within the allocated frequency band.

Figure 1.10 User Equipment Moving Between Base Stations

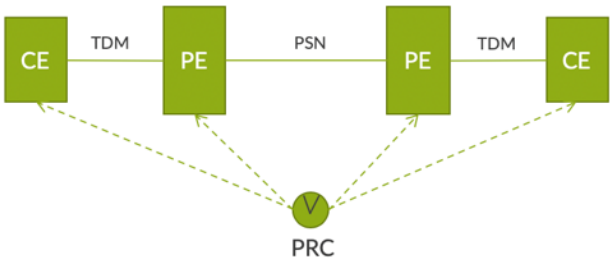


The synchronization requirement for a 2G GSM network defined by the standard is as follows:

"The BTS shall use a single frequency source of absolute accuracy better than 0.05 ppm for both RF frequency generation and clocking the timebase. The same source shall be used for all carriers of the BTS. For the pico BTS class the absolute accuracy requirement is relaxed to 0.1 ppm."

In Circuit Emulation Services (CES), the Customer Edge (CE) node and Provider Edge (PE) node should be synchronized in frequency to avoid bit-slips, which would otherwise result in under-run/over-run issues at the jitter buffer that are implemented on PEs. The main challenge here is the adoption of the TDM signal via a Packet Switched Network (PSN) and keeping the TDM clock unaffected by the Packet Delay Variation (PDV) introduced by the PSN (see Figure 1.11).

Figure 1.11 CES-CE-PE Synchronization



Universal Mobile Telecommunication System (UMTS) is a 3G cellular system based on GSM. For 3G networks, UMTS requirements are defined for Frequency Division Duplex (FDD) and Time Division Duplex (TDD) separately. The frequency error, which is the difference between the actual Base Station (BS) transmit frequency and the assigned frequency, is specified as stated here:

The modulated carrier frequency of the BS shall be accurate to within the following accuracy range [...] observed over a period of one timeslot:

Wide area BS: ±0.05 ppm

Local area BS: ±0.1 ppm

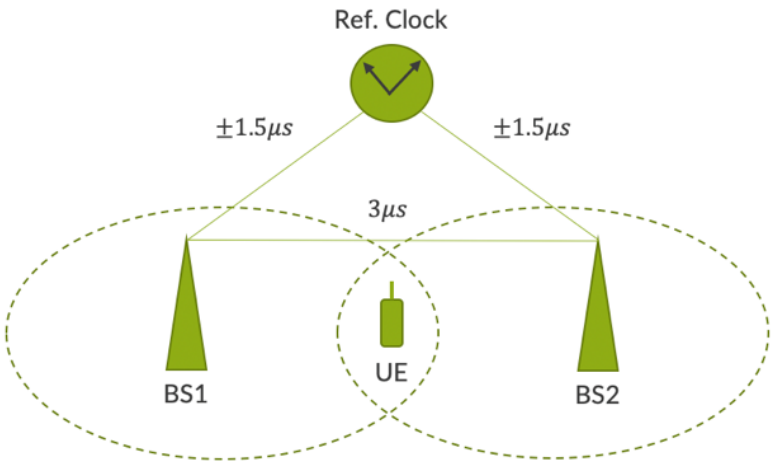
Home BS: ±0.25 ppm

The phase synchronization requirement of 3G (UMTS) is defined to accurately generate the TDD frame on the radio interface to avoid the interference between the signals generated by the adjacent base stations:

3 μs maximum deviation in frame start times between any pair of cells on the same frequency that have overlapping coverage areas.

This translates to a maximum phase error of +/-1.5μs with respect to a common absolute reference clock as shown in Figure 1.12.

Figure 1.12 3G (UMTS)-Phase Synchronization



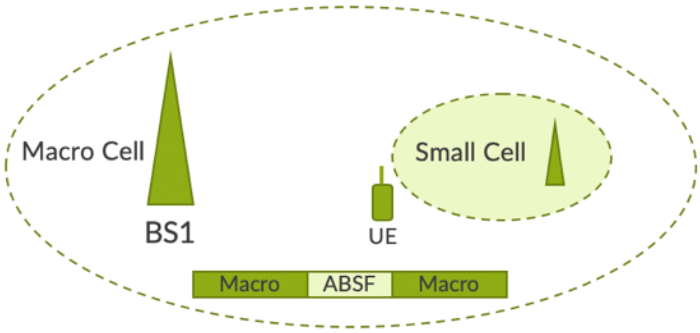
In the case of 4G-LTE (Long Term Evolution) for the TDD option, 3GPP specifies the following requirement:
"maximum absolute deviation in frame start timing between any pair of cells on the same frequency that have overlapping coverage areas"

3 μs for small cell (<3 km radius);

10 μs for large cell (>3km radius).

In heterogeneous networks, where both macro cell and small cell are deployed, coordination of the Almost Blank Sub Frame (ABSF) requires some level of frequency, phase, and time synchronization between the macro cell and the small cell (see Figure 1.13). This is to ensure that there is no misalignment of the subframe transmitted from the macro cell and small cell as received at the UE location due to the difference in propagation delays in the transmission from macro cell as compared to small cell.

Figure 1.13 Synchronization-Heterogeneous network



LTE-Advanced (LTE-A) imposes more stringent requirements for phase synchronization of 260ns for carrier aggregation technology.

5G has more stringent requirements of phase synchronization. In 5G networks, the number of distributed small cells and remote radio heads (RRH) is expected to be much higher to meet its high traffic demand. So it is expected that co-operative radio techniques such as Co-ordinated Multipoint (CoMP) and inter-site Carrier Aggregation (CA) will be deployed to deliver the high data rates required. Depending on the technique, this would require a relative phase accuracy of better than 130ns. The phase requirements of various 4G/5G applications are summarized in Table 1.1.

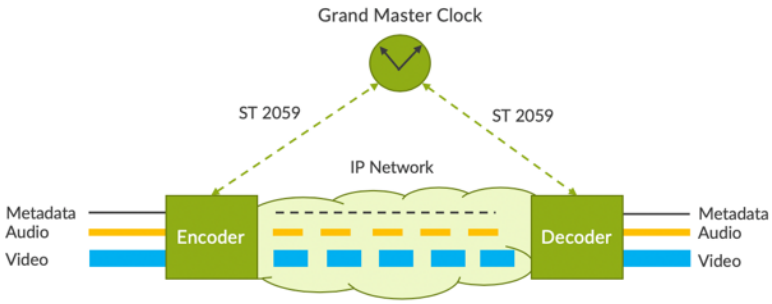
Table 1.1 Phase Requirements of 4G/5G Applications

4G/5G applications	Phase accuracy	Relative/Absolute
TDD	**+/- 1.5 *µs***	**Absolute**
Intra-band non-contiguous CA	**+/- 130 *ns***	**Relative**
Inter-band CA	**+/- 130 *ns***	**Relative**
Coordinated multi-point (CoMP) with Joint Transmission (JT)	**+/- 130 *ns***	**Relative**
eCPRI (IEEE 802.1CM)	**+/- 130 *ns***	**Relative**
Intra-band contiguous Carrier Aggregation (CA)	**+/- 65 *ns***	**Relative**
Transmit diversity Category A+	**+/- 32 *ns***	**Relative**
MIMO (category A+)	**+/- 32 *ns***	**Relative**
High accuracy positioning service (All RRU/AAU connected to same DU)	**10 *ns***	**Relative**
Self-driving/Autonomous cars	**< 5 *ns***	**Relative**

Accurate time is critical for fair and equitable financial markets. Every transaction in a financial market should be recorded with a very accurate time stamp. The accuracy of these time stamps plays an important role in deciding the financial fortune of many investors, be they small- or large-scale. With distributed computing systems, every computer system must maintain an accurate clock. This is to ensure that the first request received by the market is given precedence over the requests that arrive later. The level of accuracy required is determined both by the application and by the regulators of each market. As per the Market in Financial Instruments Directive II (MiFIDII), a European standard, the time stamp resolution requirement for High Frequency Trading (HFT) with respect to a UTC time reference is about $1\mu s$.

In professional Audio Video Bridging (AVB), the precision requirement is also around $1\mu s$ ($shown\ in\ Figure$ 1.14). This facilitates tight syncing between multiple AV streams, needed for lip syncing between video and related audio streams, to keep multiple digitally connected speakers in phase in a professional environment, and to prevent audio or video packets from arriving late to the endpoint, resulting in a dropped frame of video and unwanted audio glitches such as a pop or silence.

Figure 1.14 AVB-Synchronization



Last but not least, event or alarm correlation for specific events requires sub-second levels of accuracy. Estimation of a one-way delay as per ITU-T Y.1731 to a micro-second level of accuracy requires a common time synchronization reference at the measurement reference point.

Juniper Hardware That Supports Timing

Timing features are supported on Juniper's MX, ACX, QFX, PTX, and EX Series of network devices. These platforms are designed to cater to the needs of various market segments and use cases. Accordingly, the supported timing features may vary from platform to platform. Specific features may also vary based on the hardware capability of the platform. One such example is certain legacy mic cards that don't support MAC/PHY based-based time stamping. Such limitations due to hardware

are captured in the Notes for Tables 1.2 through 1.6. These tables provide a quick summary of the various Juniper platforms and line cards supporting timing.

NOTE Always rely on the more up-to-date versions of this information in the data sheets of these corresponding products.

Table 1.2 Juniper MX Series Supporting Timing

Product	Line Card	Interface Card
MX80-P	**MPC Built-in**	**3D 20x 1GE(LAN)- E,SFP (Note 1)**
MX104	**MPC Built-in**	**3D 20x 1GE(LAN)- E,SFP (Note 1)** **3D 20x 1GE(LAN)- EH,SFP (Note 1)** **PIC0: Built-in 4x10G SFPP (Note 1)** **MIC-3D-20GE-SFP (Note 2)**
MX204	**MPC Built-in**	**PIC0: 4XQSFP28** **PIC1: 8XSFPP**
MX240 MX480 MX960 MX2008 MX2010 MX2020	**MPC1E (Note 2)**	
	MPC2E (Note 2)	
	MPC3E	
	MPC2E NG HQoS **MPC3E NG HQoS** **MPC2E NG PQ & FlexQ** **MPC3E NG PQ & FlexQ**	**3D 20x 1GE(LAN)- E,SFP (Note 1)** **3D 20x 1GE(LAN)- EH,SFP (Note 1)** **MIC-3D-20GE-SFP (Note 2)** **MIC-3D-2XGE-XFP (Note 2)** **MIC3-3D-10XGE-SFPP (Note 2)** **MIC-3D-4XGE-XFP (Note 2)**
	MPC5E 3D 24XGE+6XLGE (Note 3) **MPC5E 3D Q 2CGE+4XGE (Note 4)**	
	MPC6E 3D (Note 4)	**24x10G SFPP OTN** **2x100G CFP2 OTN**
	MPC7E 3D 40XGE **MPC7E 3D MRATE-12xQSFPP- XGE-XLGE-CGE (Note 5)**	
	MPC8E 3D **MPC9E 3D**	**MRATE-12xQSFPP-XGE-XLGE-CGE (Note 5)**
	MPC10E 3D	
	MPC11E-3D	
MX10003	**LC2103: MRATE-12xQSFPP-XGE-XLGE-CGE (Note 5)**	**PIC0: 6xQSFPP**
MX10008	**LC2101: 24xQSFPP**	
MX100016	**LC2101: 24xQSFPP** **LC2101: 24xQSFPP (MACSEC)**	

Note 1-MIC/Ports support PHY time-stamping.

Note 2-HW time-stamping supported. PHY/MAC time-stamping not supported.

Note 3-6XLGE interface on MPC5E doesn't support PHY time-stamping. Other ports support PTP with PHY time-stamping.

Note 4-SFPP OTN MIC and CFP2 OTN MIC support PTP with PHY time-stamping.

Note 5-MRATE MIC support PTP with MAC time-stamping.

Table 1.3 Juniper ACX Series Supporting Timing

Product	Line Card	Interface Card
ACX7100-48L	**FPC Built-in**	**48x50G+6x400G**
ACX7100-32C	**FPC Built-in**	**32x100G+4x400G**
ACX6360-OR	**FPC Built-in**	**20x100/40GE** **80x10GE** **8xCFP2**
ACX5448	**FPC Built-in**	**48x1GE/10GE** **16x10/25GE 4x100/40GE**
ACX5448-M	**FPC Built-in**	**36x1/10GE** **2xCFP2** **16x10/25GE 4x100/40GE**
ACX5448-D	**FPC Built-in**	**4x100/40GE** **44x10GE**
ACX5048 ACX5096	**FPC Built-in (Note 1)**	**48x1GE/10GE** **96x1GE/10GE**
ACX710	**FPC Built-in**	**24x1/10GE** **16x10/25GE 4x100/40GE**
ACX1000	**FPC Built-in**	**8xT1/E1** **8x1GE RJ45** **4x1GE SFP Combo**
ACX1100	**FPC Built-in**	**8x1GE RJ45** **4x1GE SFP Combo**
ACX2100	**FPC Built-in**	**16xT1/E1** **6x1GE RJ45** **2x1GE RJ45-POE** **2x1GE SFP** **2x10GE SFPP**
ACX2200	**FPC Built-in**	**4x1GE RJ45** **4x1GE RJ45/SFP** **2x1GE SFP** **2x10GE SFPP**
ACX4000	**6xGE RJ45/SFP Combo** **16xT1/E1**	**8x1GE Combo** **2x1GE SFP** **2x10GE SFPP**
ACX500	**FPC Built-in (Note 2)**	**2x1GE SFP** **4x1GE RJ45/SFP**

Table 1.4 Juniper QFX Series Supporting Timing

Product	Line Card	Interface Card
QFX5100-24Q	**FPC Built-in (Note 1)**	**24x40G**
QFX5100-48S/T	**FPC Built-in (Note 1)**	**48x10G/1G+6x40G**
QFX5100-96S	**FPC Built-in (Note 1)**	**96x10G+8x40G**
QFX5110-48S	**FPC Built-in**	**48x1/10G+4x100/40G**
QFX5110-32Q	**FPC Built-in**	**28x40G+4x100/40G**
QFX5120-48Y	**FPC Built-in (Note 1)**	**48x25G/10G/1G+8x100/40G**
QFX5120-32C	**FPC Built-in (Note 1)**	**32x100G+2x10G**
QFX5120-48T	**FPC Built-in (Note 3)**	**6x100G+48x10GBaseT/1G**
QFX5200-32C	**FPC Built-in**	**32x100/40G**
QFX5210-64C	**FPC Built-in (Note 1)**	**64x100/40G+2x10G**
QFX5220-32CD	**FPC Built-in (Note 3)**	**32x400/100/40G+2x10G**
QFX5220-128C	**FPC Built-in (Note 3)**	**128x100/40G+2x10G**
QFX10002-36Q	**FPC Built-in (Note 2)**	**36x40G or 12x100G**
QFX10002-72Q	**FPC Built-in (Note 2)**	**72x40G or 24x100G**
QFX10002-60C	**FPC Built-in (Note 2)**	**60x100/40G**
QFX10008		
QFX10016		

Note 1: PTP and SyncE feature not supported due to HW limitation.

Note 2: Media/Enterprise profile features supported only on 10G interface.

Note 3: No support of PTP on 1GE out of band port.

Table 1.5 Juniper PTX Series supporting Timing

Product	Line Card	Interface Card
PTX3000 (Note 1)		
PTX5000 (Note 1)		
Note 1: SyncE feature supported.		

Table 1.6 Juniper EX Series Supporting Timing

Product	Line Card	Interface Card
EX9251	NA	8x1GE/10GE 4x40GE/100GE
EX9253-6Q12C	12x40GE/100GE QSFP28 + 6x40GE QSFP+	

Juniper Software Supporting Timing

Junos support for timing was introduced early in the 12.3 release with PTP and SyncE on the MX Series platform. The advanced PTP profile, such as G.8275.1, was introduced in the 17.1 release on the MPC5E card and subsequently on various other line cards and platforms. A multitude of timing features are currently supported on various platforms and line cards based on customer requirements and market use cases. In the ACX series of platforms, ACX710 is the first platform supporting the G.8275.1 profile. Junos EVO support for timing was introduced in the 19.4 release with a PTP Enterprise profile on the QFX5220-32CD platform and, subsequently, the end-to-end transparent clock feature on 20.1 release. Please refer to the release-specific technical documentation for additional information on specific feature availability on various platforms.

MORE? As Juniper provides timing features on an increasing number of products, use the Feature Explorer to obtain the most up-to-date information beyond what you may see in this book: https://apps.juniper.net/feature-explorer/.

Summary

This chapter provided an overview of synchronization and its requirements in various applications and technologies, and it summarized the various Juniper hardware platforms supporting timing features along with the applicable known hardware limitations. It also provided an overview of Junos (and Junos EVO) timing support on various platforms with appropriate references. Now let's start analyzing how it all works together.

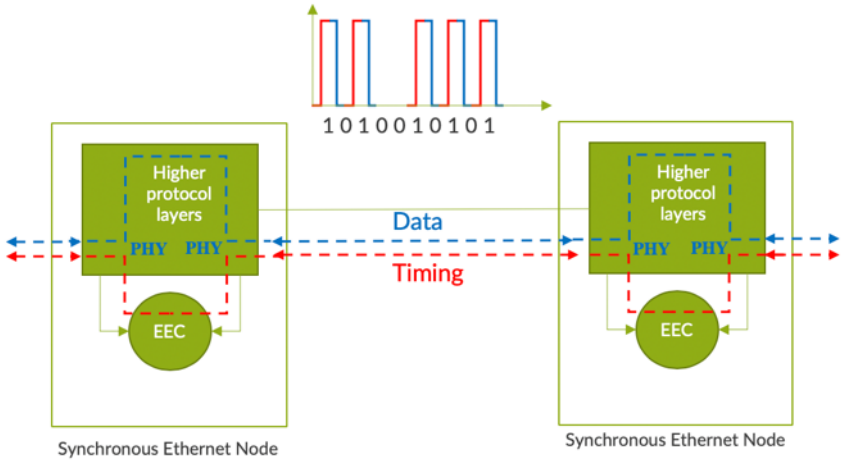
Chapter 2

Synchronous Ethernet

What is Synchronous Ethernet?

Synchronous Ethernet (SyncE) transmits frequency over communication links at the physical layer, similar to synchronization based on E1/T1, Synchronous Optical Networks (SONET), and Synchronous Digital Hierarchy (SDH). Figure 2.1 illustrates the clock recovery in Synchronous Ethernet from an incoming "bit stream."

Figure 2.1 Basic Clock Recovery in Synchronous Ethernet



The clock recovered from incoming data is usually fed to a Phase Locked Loop (PLL) to smooth it out and send it to a downstream node. Optionally, this clock can drive the chassis clock of the node at which it is extracted, and fan-out the clock on all its SyncE-supported interfaces. SyncE forms a chain (or tree) of interconnected Ethernet Equipment Clocks (EECs) whose sources can be traced to a Primary Reference Clock (PRC). So, in Figure 2.1, the clock received by the left side node will ultimately be received from a PRC assuming no failures along the path.

The main advantage of Synchronous Ethernet is that the accuracy of the frequency recovered is independent of network load, and hence SyncE is very accurate, while a limitation of Synchronous Ethernet is that it can only carry frequency, not phase information; it also requires end-to-end Synchronous Ethernet connectivity.

ESMC Messages

SyncE, similar to SONET/SDH, supports a Synchronization Status Message (SSM) like mechanism to send synchronization signals along the tree or chain of EECs. This is called an Ethernet Synchronous Messaging Channel (ESMC) in the realm of SyncE. The ESMC carries information about the quality of the clock, known as quality level (QL), from the source, to all the clocks along the branches of the SyncE clock hierarchy. Therefore it is very important to determine the traceability of the clock. If the selected clock in the upstream network element (NE) fails, a new clock will be selected based on the QL values and configured priorities. One of the main goals of ESMC is to help prevent timing loops. A proper network design is a must, however, to prevent the timing loops for certain specific scenarios.

Two types of messages are defined for SyncE: *general message/information* and *event* messages. The event flag mentioned in the ESMC PDU specifies the message type. Typically, the general message is transmitted once a second and the event message is transmitted immediately when there is a change of the clock QL.

The ESMC PDU format as per ITU-T G.8264 mentioned in Table 2.1a is for both information and event messages. The length field encompasses the entire TLV, including the type and length fields. To allow for potential hardware implementations, the SSM TLV is always sent as the first TLV in the data/padding field. This means that the QL indication always remains fixed in the PDU. Any padding must occur after the SSM TLV. The SSM code is a 4-bit field, which maps to the corresponding ESMC-QL value per Table 2.1b and Table 2.1c. For a ESMC packet decode refer to the Appendix.

Table 2.1a ESMC PDU format

Size	Field
6 octets	**DA=01-80-c2-00-00-02**
6 octets	**SA**
2 octets	**Slow protocol Ether-type=88-09**
1 octet	**Slow protocol subtype=0x0A**
3 octets	**ITU-OUI=00-19-A7**
2 octets	**ITU-T subtype**
4 bits	**version**
1 bit	**Event Flag**

3 bits	**Reserved**
3 octets	**Reserved**
4 octets	**TLV**
32-1486 octets	**Future Enhancement TLV**
4 octets	**FCS**

Table 2.1b ESMC QL TLV

Size	ESMC QL TLV
8 bits	**Type: 0x01**
16 bits	**Length: 0x00-04**
4 bits	**0x0 (unused)**
4 bits	**SSM Code**

Table 2.1c Extended ESMC QL TLV

Size	Extended ESMC QL TLV
8 bits	**Type: 0x02**
16 bits	**Length: 0x00-14**
8 bits	**Enhanced SSM Code**
64 bits	**SyncE clockIdentity of the originator of the extended QL-TLV**
8 bits	**Flag**
8 bits	**Number of cascaded eEECs from the nearest SSU/PRC/ePRC**
8 bits	**Number of cascaded EECs from the nearest SSU/PRC/ePRC**
40 bits	**Reserved for future use**

Table 2.1d ESMC QL Values-Network Option-1

Network Option-1 as per ITU-T G.8264

ESMC QL	SSM Code	Enhanced SSM Code
PRC	**0010**	**0xFF**
SSU-A	**0100**	**0xFF**
SSU-B	**1000**	**0xFF**

SEC/EEC1	**1011**	**0xFF**
DNU	**1111**	**0xFF**
PRTC	**0010**	**0x20**
ePRTC	**0010**	**0x21**
eEEC	**1011**	**0x22**
ePRC	**0010**	**0x23**

Table 2.1e ESMC QL Values-Network Option-2

Network Option-2 as per ITU-T G.8264

ESMC QL	SSM Code	Enhanced SSM Code
PRS	**0001**	**0xFF**
STU	**0000**	**0xFF**
ST2	**0111**	**0xFF**
TNC	**0100**	**0xFF**
ST3e	**1101**	**0xFF**
ST3/EEC2	**1010**	**0xFF**
PROV	**1110**	**0xFF**
DUS	**1111**	**0xFF**
PRTC	**0001**	**0x20**
ePRTC	**0001**	**0x21**
eEEC	**1010**	**0x22**
ePRC	**0001**	**0x23**

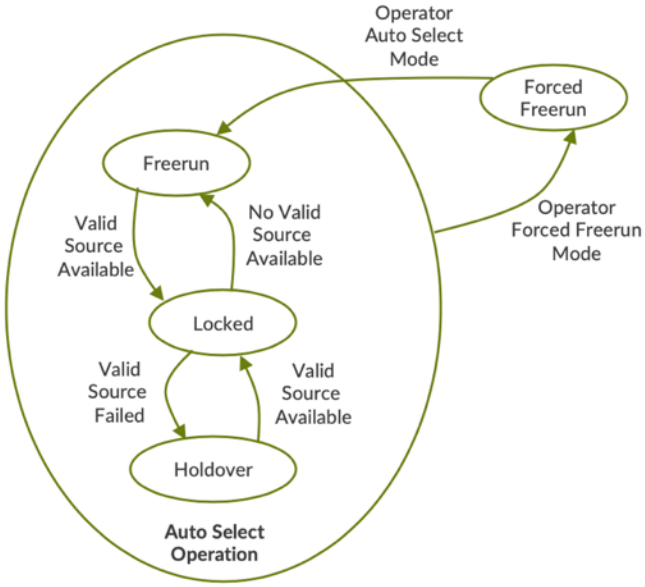
Clock Selection Algorithm

In SyncE devices, the clock selection supports two modes of operation:

- Forced free-run
- Automatic selection

Default operational mode is forced freerun. In this case the local OCXO is selected as the chassis clock source. The automatic selection operation runs in free-run until a valid source is qualified and the source is selected. Once the source is selected, up to 60 seconds is required for the clock module to acquire lock, and once locked, holdover data is collected in the history buffer. If a locked reference QL drops below the threshold, or a fail condition signal occurs, holdover mode is entered until another valid source is found, as in the clock selection state-machine in Figure 2.2.

Figure 2.2 Clock Selection State-machine



In the automatic clock selection process, the operator selects a number of physical ports as potential sources for candidate synchronization. Each port is assigned a priority where the configured values can range from 1 to 5, 1 being the highest priority and 5 being the lowest priority. The primary and secondary clock source will be selected based on the quality and priority of each clock source.

Automatic clock selection generally operates in two modes:

- Quality mode enabled
- Quality mode disabled

In QL enabled mode, best clocks are selected based on the incoming ESMC QL, as long as the incoming QL is at least as good as the source's

configured QL. If the QLs are equal, then clock selection takes place based on a user-configured priority. If both received QLs and priority are equal, then one of the sources is selected randomly. The following Junos knobs enable QL mode and selection-mode received quality:

```
selection-mode received-quality
quality-mode-enable
```

However, you can also configure `selection-mode configured-quality` in QL enabled mode with the following commands (the best clocks are selected based on the configured ESMC QL, and the selected configured ESMC is advertised in the downstream direction):

```
selection-mode configured-quality;
quality-mode-enable;
```

A few reasons for using `configure-quality` when operating in QL Enabled mode is to:

- Interface with old equipment that does not support SSM or ESMC generation;
- Interface with equipment operating in the QL-disabled mode;
- Select an interface that does not support SSM/ESMC processing;
- Or, select signals for which SSM is not defined (2/5/10 MHz signals).

NOTE Juniper supports the `no-ssm-support` option at the `[show chassis synchronization source interface]` hierarchy level to handle scenarios in which one interface does not support ESMC-QL and the other interface supports ESMC-QL with `selection-mode received-quality`. This enables both interfaces to participate in clock selection algorithms.

In QL disabled mode the best clocks are always selected based on user configured ESMC QLs. If the QLs of the best clocks are equal, then the clock selection takes place based on a user-configured priority. If both the user-configured QLs and priority are equal, then it randomly selects one or the other.

To prevent the selection algorithm from running before the SSM-QL has been learned, there is a configurable selection hold-off time that must elapse before the clock selection algorithm is run.

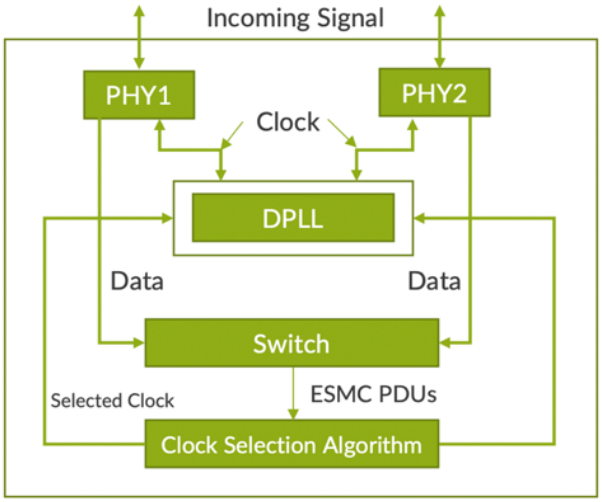
The Clock Selection Algorithm (CSA) plays a major role in topology synchronization and timing-loop prevention since it allows automatic reconfiguration in case of link failure. However, it is the responsibility of the operator to configure ESMC correctly while effectively preventing timing loops.

The CSA can be triggered by the following events:

- Signal failure detected on currently selected source.
- Changes in ESMC QLs received.
- User configuration changes (addition/deletion of a clock source, QL Enable mode changed, etc.)

Figure 2.3 depicts a high-level block diagram of clock selection.

Figure 2.3 Clock Selection-block Diagram



Usually, the PHY detects the clock, and the clock module continuously monitors references for frequency accuracy and phase regularity. If the clock quality is within the DPLL hold-in range, which is +/- 4.6 ppm, it qualifies the clock based on the clock selection algorithm using ESMC-QL values. This means a reference fails clock qualification if the measured frequency exceeds 9.2 ppm.

Configuring and Verifying SyncE

Let's now configure each of SyncE's parameters in Junos in order to provide a consistent and flexible SyncE design.

Before We Begin

In this section's artwork you'll see numbers labeled as 1, 2, 3, etc., and enclosed in circles, which are the network interface numbers; this convention is used throughout the book. For example, if the number is 1, 2, or 3, then the actual port number would be:

1 = xe-0/0/1

2 = xe-0/0/2

3 = xe-0/0/3, and so on.

Also used are the notations West (W) and East (E) to represent the west and east interface of the node. Throughout this book, Paragon-x is used as the clock tester. You can use any other test devices you wish with similar capabilities.

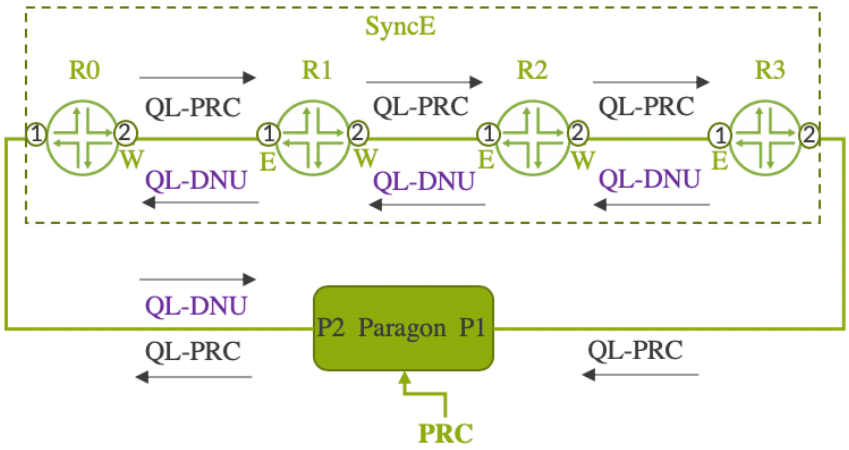
There is no single common topology used in this book. Based on the technology, use cases, and from the point of view of illustration, multiple topologies are used instead. Your own network will, of course, be unique. If you can build a follow-along test bed mimicking our simple topologies, you should be able to closely follow along as a lab exercise.

NOTE For proper validation of Synchronous Ethernet, the most important requirement is a valid reference clock and a Tester which uses this external source as the reference clock. The reference clock PRC can be derived from the stratum-1 source such as GPS, or any other clock source, such as Rubidium, which provides a stable clock. Paragon is used in the book as the clock tester.

NOTE Throughout this book, we have used `network-option-1` for all configurations. You can change the configurations based on your requirements. Please refer the Table 2.1d and Table 2.1e for QL values for both options.

Unidirectional Linear Chain

Figure 2.4 Unidirectional Linear Chain



In Figure 2.4, the role of the PRC is to provide an accurate reference to the tester, and, it is also used for comparing a measured signal to the reference signal. This reference is usually derived from GPS. So the tester generates a proper clock with its associated ESMC QL, QL-PRC to the device R0. Device R0 recovers the clock on xe-0/0/1 and transmits the recovered clock to R1. Now let's look at the configuration on R0. It is notable that the second interface xe-0/0/2 is not configured as source for chassis clock, as we don't expect any clock from the upstream.

Example 2.1 Configuration of chassis synchronization on R0

```
1         user@R0# run show configuration chassis synchronization
2         network-option option-1;
3         selection-mode received-quality;
4         quality-mode-enable;
5         source {
6             interfaces xe-0/0/1 {
7                 priority 1;
8                 wait-to-restore 0;
9                 quality-level prc;
10            }
11        }
12        esmc-transmit {
13            interfaces all;
14        }
```

Since the configuration has `quality-mode-enable` and `selection-mode received-quality`, R0 transmits the recovered clock with ESMC QL-PRC to R1 and device R1, recovers the clock on xe-0/0/1, and sends the clock further down the chain where device R3 finally transmits the recovered clock towards port P1 of the tester.

The knob `quality-level prc` (line number 9) is the configured quality and the command `esmc-transmit interfaces all` (line numbers 12-13) enables R0 to advertise the received quality via all the configured IFLs, which are operationally up. If you want to enable `esmc-transmit` on a selected IFL, then specify those specific IFLs under the `esmc-transmit` knob as `esmc-transmit interfaces xe-0/0/2.0`.

Let's see now how we verify Synchronous Ethernet on device R0. Thanks to the configuration on R0, it's locked to the external clock source.

Example 2.2 Output of chassis synchronization on R0

```
1         user@R0# run show chassis synchronization extensive
2         Current clock status  : Locked
3         Clock locked to       : Primary
4         SNMP trap status      : Disabled
5         Configured sources:
6         Interface           : xe-0/0/1
7         Status              : Primary       Index       : 160
8         Clock source state  : Clk qualified Priority    : 1
9         Configured QL       : PRC           ESMC QL     : PRC
10        Clock source type   : ifd           Clock Event : Clock locked
11        Wait-to-restore     : 0  min        Hold-off    : 1000 ms
12        Interface State     : Up,pri,ESMC Rx(SSM 0x2),ESMC TX(QL DNU/SSM 0xf),
```

The `Current clock status` (line number 2) in the output indicates that the clock module on R0 is `Locked` to the specific clock source. However, in case the clock source is invalid, the `Current clock status` can assume other states as diagrammed in Figure 2.2. Freerun is the default state of the clock module.

The interface xe-0/0/1 is selected as Primary (line number 7). The default `Hold-off` time is 1000 ms (line number 11), and you can configure the `Hold-off` time for each port. When a port signal transitions into the signal fail state, the `Hold-off` time must elapse before the selection process is notified of the signal failure. The `Hold-off` time range is 300 ms to 1800 ms.

Similarly, the default value for `wait-to-restore` time is 5 minutes. A `wait-to-restore` time can be configured for each port. When a port signal transitions out of the signal fail state, it must be fault free for the duration of `wait-to-restore` time before it is again considered by the selection process. The `wait-to- restore` time is configurable in the range of 0 to 12 minutes in one minute increments. The `wait-to-restore` timer can be cleared with the separate clear command. If the timer is cleared, the new QL and the cleared signal fail state are immediately passed to the selection process.

It is important to note that Junos (and Junos EVO) have default values set for `synchronous-ethernet global-information`. The configuration parameters shown in Example 2.3 are enabled by default.

Example 2.3 Output of global-information on R1

```
1        user@R1# run show synchronous-ethernet global-information
2        Global Configuration:

3        Network option         : option-1(EEC1)
4        Clock mode             : Auto-select
5        Max transmit quality   : PRC
6        QL mode                : Enabled
7        Clock selection mode   : Receive-QL based
8        Switchover mode        : Revertive
9        Config change holdover : 15  seconds
10       Switchover holdover    : 30  seconds
11       Reboot holdover        : 120 seconds
12       RE Status              : Master
13       Global Wait to Restore : 5   min
```

You can override these values using Examples 2.4 and 2.5.

Example 2.4 Configuration of hold-interval on R1

```
1        user@R1# set chassis synchronization hold-interval ?
2        Possible completions:
3        configuration-change  Clock select wait time after change in config (15..60 sec)
4        restart               Clock select wait time after reboot (60..180 sec)
5        switchover            Switchover wait time after clock recovery (30..60 sec)
```

Example 2.5 Configuration of global-wait-to-restore time on R1

```
1        regress@R1# set chassis synchronization global-wait-to-restore ?
2        Possible completions:
3          <global-wait-to-restore>  Global Port signal up state time before opening for ESMC 4
         (0..12 min)
```

Let's look at the chassis synchronization configuration on R1, R2, and R3.

These configurations are almost the same as that of R0. You will need to change the configured source interface if required. There is nothing that prevents you from configuring the lower QL value as the configured quality-level. As discussed earlier, as long as the received QL is equal to or better than the configured one, we're good.

Example 2.6 Configuration of chassis synchronization on R1

```
1         user@R1# run show configuration chassis synchronization
2         network-option option-1;
3         selection-mode received-quality;
4         quality-mode-enable;
5         source {
6             interfaces xe-0/0/1 {
7                 priority 1;
8                 wait-to-restore 0;
9                 quality-level prc;
10            }
11        }
12        esmc-transmit {
13            interfaces all;
14        }
```

Example 2.7 Configuration of chassis synchronization on R2

```
1         user@R2# run show configuration chassis synchronization
2         network-option option-1;
3         selection-mode received-quality;
4         quality-mode-enable;
5         source {
6             interfaces xe-0/0/1 {
7                 priority 1;
8                 wait-to-restore 0;
9                 quality-level prc;
10            }
11        }
12        esmc-transmit {
13            interfaces all;
14        }
```

Example 2.8 Configuration of chassis synchronization on R3

```
1         user@R3# run show configuration chassis synchronization
2         network-option option-1;
3         selection-mode received-quality;
4         quality-mode-enable;
5         source {
6             interfaces xe-0/0/1 {
7                 priority 1;
8                 wait-to-restore 0;
9                 quality-level prc;
10            }
11        }
12        esmc-transmit {
13            interfaces all;
14        }
```

Let's issue the command to verify the SyncE lock status as specified in Example 2.9. It's evident from the output that R3 is locked to the upstream device R2 and the selected interface is xe-0/0/1. The `Interface State` (line 12) in the below output clearly indicates that the selected interface has

received Rx(SSM 0x2), which means PRC and hence the Tx QL is DNU.

Example 2.9 Output of chassis synchronization on R3

```
1         user@R3# run show chassis synchronization extensive
2         Current clock status  : Locked
3         Clock locked to       : Primary
4         SNMP trap status      : Disabled
5         Configured sources:
6         Interface           : xe-0/0/1
7         Status              : Primary       Index       : 160
8         Clock source state  : Clk qualified Priority    : 2
9         Configured QL       : PRC           ESMC QL     : PRC
10        Clock source type   : ifd           Clock Event : Clock locked
11        Wait-to-restore     : 0  min        Hold-off    : 1000 ms
12        Interface State     : Up,pri,ESMC Rx(SSM 0x2),ESMC TX(QL DNU/SSM 0xf),
```

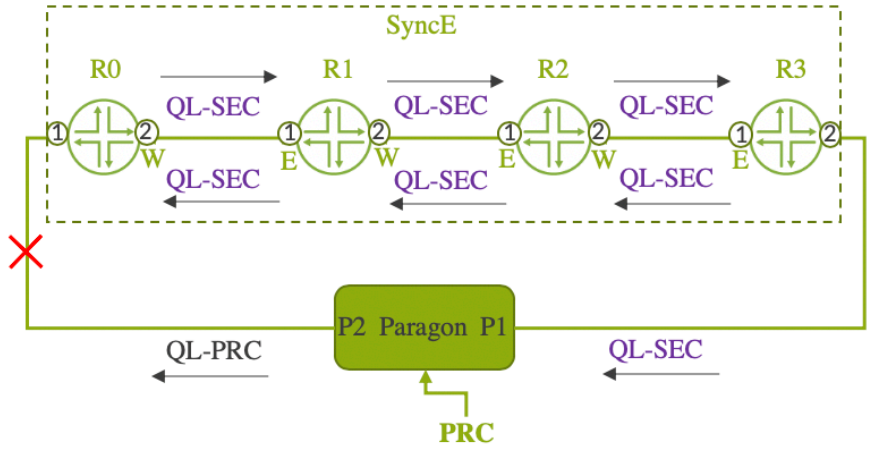
As seen in line number 12, R3 advertises ESMC QL-DNU towards its upstream source from which it recovers the clock. This is to inform the upstream Do Not Use its clock, which otherwise can lead to a timing loop. So QL-PRC flows from West to East direction in the topology, whereas QL-DNU flows from East to West. The ESMC transmit detail can also be retrieved by using Example 2.10.

Example 2.10 ESMC transmit detail on R3

```
1         user@R3# run show synchronous-ethernet esmc transmit detail
2         ESMC Transmit interface details:
3             Interface name: xe-0/0/1          Status: ESMC Tx (QL DNU/SSM 0xf)
4             Interface name: xe-0/0/2          Status: ESMC Tx (QL PRC/SSM 0x2)
```

In case of a failure in the chain, say the link between tester and R0 is down, all devices in the chain go to holdover mode. During the holdover mode, devices send out QL-SECs on all their configured IFLs as depicted in Figure 2.5.

Figure 2.5 Unidirectional Linear Chain-Link Fail-over



NOTE If the `selection-mode` option at the `[show chassis synchronization]` hierarchy level is set to `configured-quality`, then the configured quality for the selected active source is used as the system ESMC quality level value that is transmitted out. But if the `selection-mode` option at the `[show chassis`

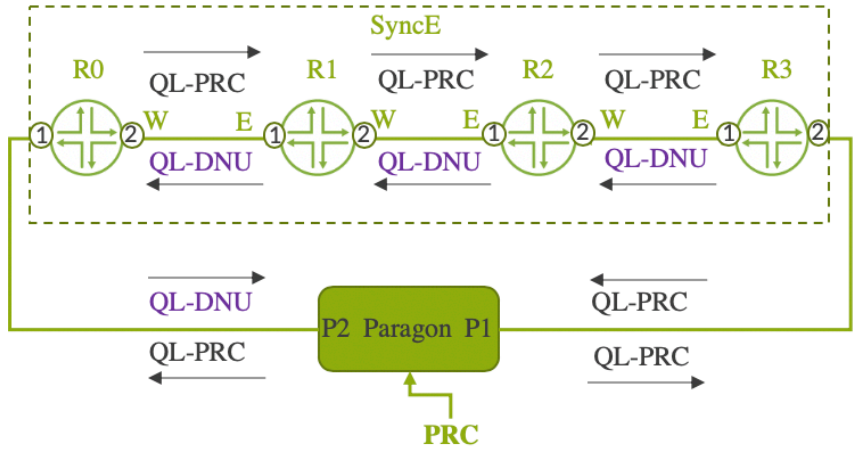
`synchronization]` hierarchy level is set to `received-quality`, then the received ESMC QL value from the selected source is transmitted out.

Now the question might arise, how long can the SyncE chain extend? Per G.8261, the PRC is connected by a chain of twenty EECs until they get to the SSUs. SSU is a clean-up clock. Then there can be another mixed chain of SECs and EECs, followed by another SSU. In total, the reference chain can consist of up to 10 SSUs and 60 EECs.

Bidirectional Linear Chain of EECs

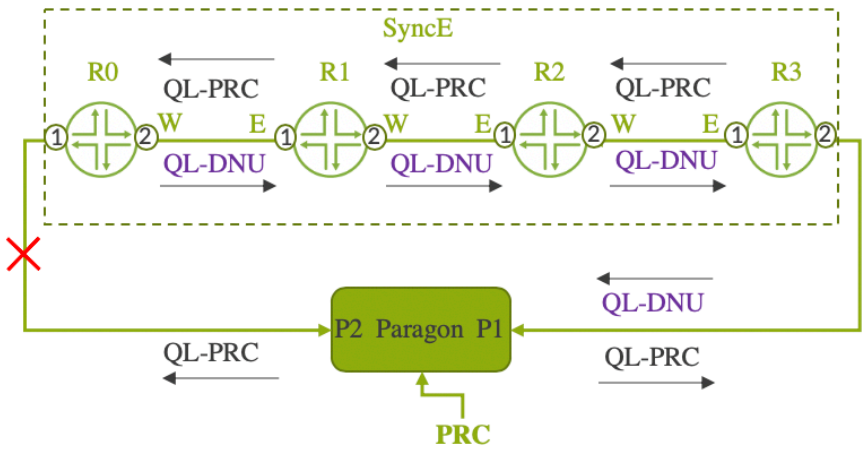
In Figure 2.6, both R0 and R3 are externally timed. This is simulated by connecting both port P2 and port P1 of the tester to R0 and R3, respectively. The priorities 1 and 2 are configured on R0 through R3 such that, under normal scenarios, the PRC connected to the R0 drive completes the SyncE chain.

Figure 2.6 Bidirectional Linear Chain



If the link between R0 and the tester's port P2 fails, the port P1 of the tester connected to R3 will drive the synchronization chain from R3 to R0, without causing any timing loops. The failover is depicted in Figure 2.7.

Figure 2.7 Bidirectional Linear Chain-Link Fail-over



The complete configurations are furnished below. In this scenario you should configure both East and West interfaces under the `chassis synchronization` source configuration with appropriate priorities. You can see in the following examples that the East interface is configured with high priority 1 and the West interface is configured with lower priority 2.

Example 2.11 Configuration of chassis synchronization on R0

```
user@R0# run show configuration chassis synchronization
network-option option-1;
selection-mode received-quality;
quality-mode-enable;
source {
    interfaces xe-0/0/1 {
        priority 1;
        wait-to-restore 0;
        quality-level prc;
    }
    interfaces xe-0/0/2 {
        priority 2;
        wait-to-restore 0;
        quality-level prc;
    }
}
esmc-transmit {
    interfaces all;
}
```

Example 2.12 Configuration of chassis synchronization on R1

```
user@R1# run show configuration chassis synchronization
network-option option-1;
selection-mode received-quality;
quality-mode-enable;
source {
    interfaces xe-0/0/1 {
        priority 1;
        wait-to-restore 0;
        quality-level prc;
    }
    interfaces xe-0/0/2 {
        priority 2;
        wait-to-restore 0;
        quality-level prc;
    }
}
esmc-transmit {
    interfaces all;
}
```

Example 2.13 Configuration of chassis synchronization on R2

```
user@R2# run show configuration chassis synchronization
network-option option-1;
selection-mode received-quality;
quality-mode-enable;
source {
    interfaces xe-0/0/1 {
        priority 1;
        wait-to-restore 0;
        quality-level prc;
    }
    interfaces xe-0/0/2 {
        priority 2;
```

```
13                wait-to-restore 0;
14                quality-level prc;
15            }
16        }
17        esmc-transmit {
18            interfaces all;
19        }
```

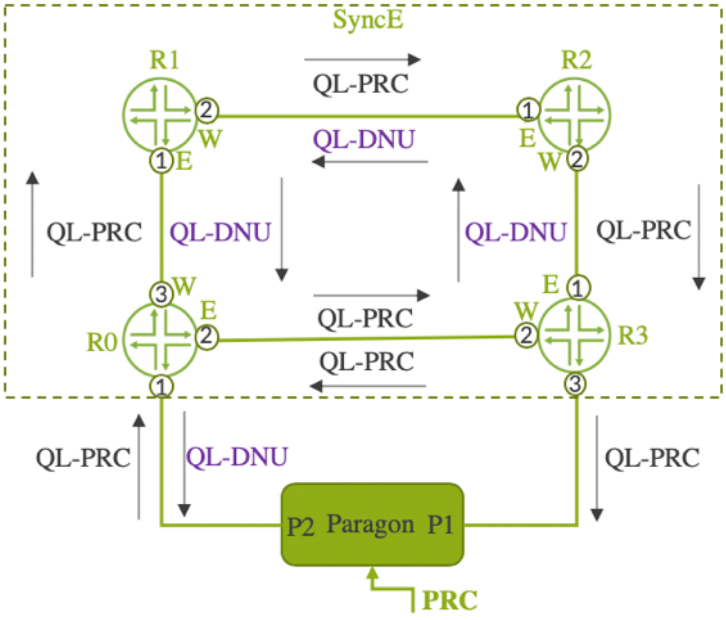
Example 2.14 Configuration of chassis synchronization on R3

```
1         user@R3# run show configuration chassis synchronization
2         network-option option-1;
3         selection-mode received-quality;
4         quality-mode-enable;
5         source {
6             interfaces xe-0/0/1 {
7                 priority 1;
8                 wait-to-restore 0;
9                 quality-level prc;
10            }
11            interfaces xe-0/0/2 {
12                priority 2;
13                wait-to-restore 0;
14                quality-level prc;
15            }
16        }
17        esmc-transmit {
18            interfaces all;
19        }
```

Ring Network with External Clock Source

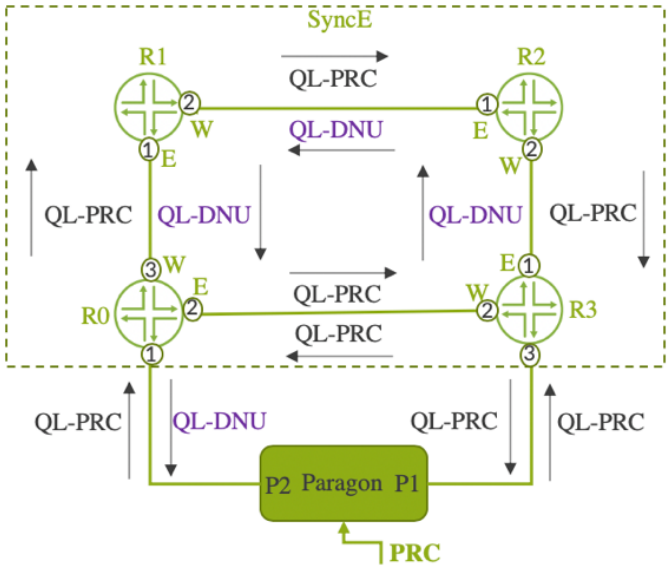
Figure 2.8 illustrates an example of a ring topology with a single external source connected to R0 on port xe-0/0/1. The port on R0 connected to tester port P2 is configured with chassis source priority 1. The west interface of the device R1 through R3 is configured with priority 2 and their east interface is configured with priority 1.

Figure 2.8 Ring Network with One External Clock Source



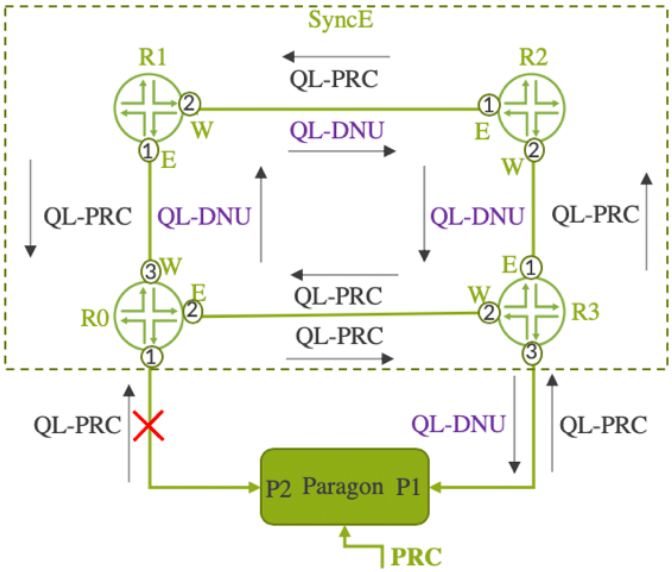
This ring can restore the synchronization when failure occurs on any of the links between R0 - R3. However, if the link connecting R0 to the tester fails, then all of the devices go into a state of holdover. To provide additional redundancy, let's configure the tester to drive the clock towards R3 as well. This simulates the case of ring topology with two external clock sources as shown in Figure 2.9.

Figure 2.9 Ring Network with Two External Sources



When there is no failure in any part of the topology, the clock propagation is similar to that discussed in the case of a ring with single external source. So we have additionally configured the priority 2 on R3 interface facing towards the tester. This will help R3 select the clock from the tester if the link from R0 to the tester fails as shown in Figure 2.10.

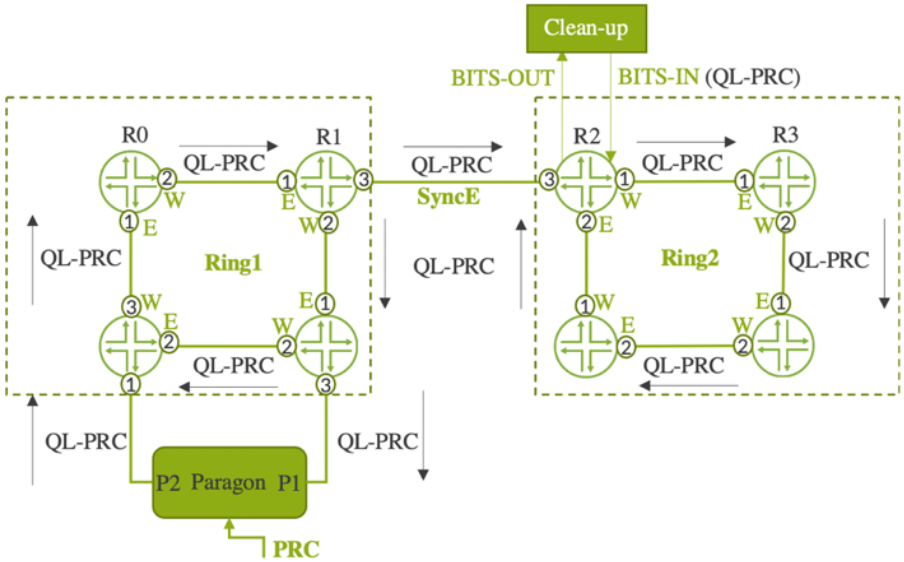
Figure 2.10 Ring Network with Two External Sources-Link Failover



Synchronization from Ring1 to Ring2 - Ring Interconnect

In Figure 2.11, Ring1 and Ring2 are co-located, but Ring2 doesn't have a separate external clock source – it depends on the clock from Ring1. For the sake of illustration only four nodes are depicted in the ring, but in reality, each ring consists of many nodes.

Figure 2.11 Ring Interconnect Network



As the number of nodes in the network increases, the wander accumulation also increases. So it is important to clean-up the signal. Typically, clean-up is recommended after every twenty EECs. In this case, we clean up the clock on R2 in Ring2 by sending the clock to a clean-up unit, typically an SSU clock with a very low bandwidth via BITS-OUT interface. R2, in turn, recovers the cleaned-up clock via its BITS-IN interface and supplies the clock to the entire Ring2. This requires a line-timing configuration on the BITS-OUT on R2 so that the incoming SyncE clock drives the BITS-OUT clock. The SyncE clock in this case must be configured as a secondary clock to R2 whereas the BITS-IN must be as primary.

NOTE Building Integrated Timing System (BITS) is a station clock with external inputs to the node for the purpose of generating node clock references. BITS supports two station clock inputs in DS1 (1.544 Mbps) and E1 (2.048 Mbps) format. Junos also supports 2.048MHz clock input. For DS1 timing reference signals, both sf and esf formats are supported. For the E1 interfaces, both g704 and g704-no-crc4 frame formats are supported. BITS also support station clock output interfaces. The output DS1 or E1 signals timed from line synchronization sources. SSM capability is supported on both station clock input and output.

NOTE BITS interface supports configurable line-coding for both signal types. For the DS1 signal, ami and b8zs line-coding is supported. For the E1 signal, ami and hdb3 line-coding is supported.

It's also possible that the Ring1 may be a legacy SONET/SDH based network and Ring2 may be the SyncE network and vice-versa. In this case, the BITS-OUT interface of R1 of Ring1 can be connected to the BITS-IN interface of R2 of Ring2. Proper synchronization design may not allow such bi-directional links controlled by SSM to avoid the risk of creating timing loops in the network.

Now let's look at the command-line configurations on R1 of Ring1 and R2 of Ring2. The `signal-type` in Line number 7 of Example 2.15 signifies the type of signal carried by the BITS interface and line numbers 12 through 16 represent the BITS output configuration.

Example 2.15 Configuration of chassis synchronization on R1

```
1       user@R1# run show configuration chassis synchronization
3       network-option option-1;
4       selection-mode received-quality;
5       quality-mode-enable;
6       interfaces external-0/0 {
7           signal-type e1;
8           e1-options {
9               framing g704;
10         }
11      }
12      output {
13          interfaces external-0/0 {
14              wander-filter-disable;
15              source-mode chassis;
16              minimum-quality prc;
17          }
18      }
19      source {
20          interfaces xe-0/0/1 {
21              priority 1;
22              wait-to-restore 0;
23              quality-level prc;
24          }
25          interfaces xe-0/0/2 {
26              priority 2;
27              wait-to-restore 0;
28              quality-level prc;
29          }
30      }
31      esmc-transmit {
32          interfaces all;
33      }
```

Example 2.16 Configuration of chassis synchronization on R2

```
35      user@R2# show chassis synchronization
36      network-option option-1;
37      selection-mode received-quality;
38      quality-mode-enable;
39      interfaces external-0/0 {
40          signal-type e1;
41          e1-options {
42              framing g704;
43              sabit 4;
44          }
```

```
45      }
46      output {
47           interfaces external-0/0 {
48              wander-filter-disable;
49              source-mode line;
50              minimum-quality prc;
51          }
52      }
53      source {
54          interfaces external-0/0 {
55              priority 1;
56              wait-to-restore 0;
57              quality-level prc;
58          }
59          interfaces xe-0/0/1 {
60              priority 2;
61              wait-to-restore 0;
62              quality-level prc;
63          }
64      }
65      esmc-transmit {
66          interfaces all;
67      }
```

Now let's look at the line numbers 46–50 of Example 2.16. Here the `source-mode line` indicates that the BITS-OUT is line-timed. However, line numbers 53 - 57 represent the configuration for BITS-IN, which is configured as a high priority source (`priority 1`) compared to SyncE source (`priority 2`).

The BITS configuration above is valid for the MX platform only. The naming convention for the BITS interface is slightly different on various Juniper platforms. The CLI configuration knob for the BITS interface for various Juniper platforms is listed in Table 2.2.

Table 2.2 BITS Interface Naming

Platform	BITS Interface naming	
	RE0/SCB0	**RE1/SCB1**
MX240/MX480/MX960 with SCBE	**external**	**external**
MX240/MX480/MX960 with SCBE2	**external-0/0**	**external-1/0**
MX2010/MX2020	**external-a, external-b**	**external-a, external-b**
MX2008	**external-0, external-1**	**external-0, external-1**
MX204/MX10003	**external-0/0**	**external-1/0**
MX10008/MX100016	**external-0, external-1**	**external-0, external-1**
ACX2100, ACX4000, ACX710	**bits**	**NA**

Some notes on the platform support:

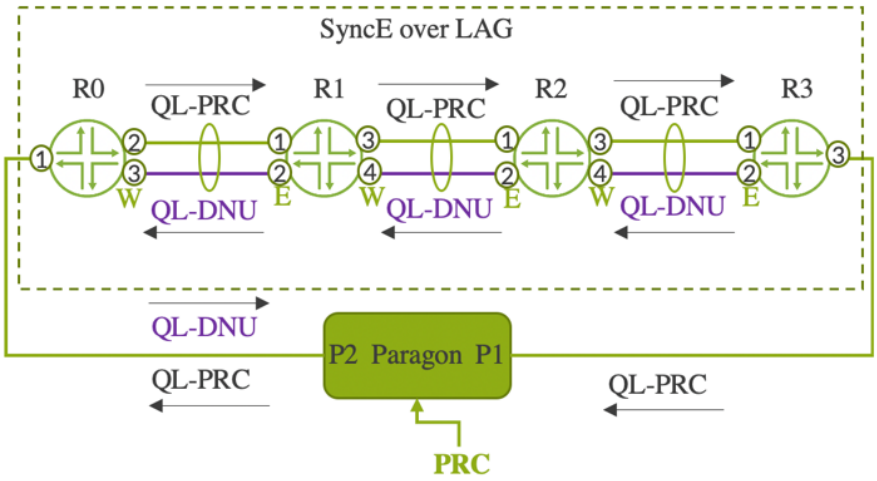
- The MX platform with SCBE3 doesn't support BITS clocking.
- As of the writing this book, the ACX710 platform supports only BITS-OUT. The E1 BITS output with g704-no-crc4 framing options works only without `quality-mode-enable` feature on ACX710.

Configuration of two bi-directional chains in parallel can lead to timing-loops. So a proper synchronization plan is needed to avoid such issues. Configuring one of the parallel links for transporting synchronization in both directions is recommended.

Synchronous Ethernet Over Link Aggregation Group

Even in Synchronous Ethernet over LAG in Figure 2.12, there is a possibility of a potential timing loop because the member links in the aggregated bundle are parallel links between two devices.

Figure 2.12 SyncE over LAG



So the algorithm is modified to send QL-DNU on all other member links as soon as any of the member ports, which are part of the LAG bundle, are selected for synchronization. For example, if the device R1 selects the first member link xe-0/0/1 as the clock source on its east interface, it transmits QL-DNU to all other members that constitute the same link aggregation group. This is true for the other devices, R2 through R3. This way the possibility of timing loops is completely avoided. Now let's look at the sample configuration on R0 which enables SyncE over LAG.

Example 2.17 Configuration of chassis synchronization over LAG on R1

```
regress@R1# show chassis
aggregated-devices {
    ethernet {
        device-count 5;
    }
}
network-services enhanced-ip
```

```
8         synchronization {
9             network-option option-1;
10            selection-mode received-quality;
11            quality-mode-enable;
12            source {
13                interfaces xe-0/0/1 {
14                    priority 1;
15                    wait-to-restore 0;
16                    aggregated-ether ae0;
17                    quality-level prc;
18                }
19                interfaces xe-0/0/2 {
20                    priority 1;
21                    wait-to-restore 0;
22                    aggregated-ether ae0;
23                    quality-level prc;
24                }
25            }
26            esmc-transmit {
27                interfaces all;
28            }
29        }
```

Note that the lines 16 and 22 in Example 2.17 are mandatory for SyncE configuration over LAG. The fact that all member links transmit QL-DNU towards the remote LAG member peers is evident in Example 2.18 (lines 3 and 4).

Example 2.18 ESMC transmit detail on R1

```
1         user@R1# run show synchronous-ethernet esmc transmit detail
2         ESMC Transmit interface details:
3             Interface name: xe-0/0/1          Status: ESMC Tx (QL DNU/SSM 0xf)
4             Interface name: xe-0/0/2          Status: ESMC Tx (QL DNU/SSM 0xf)
5             Interface name: xe-0/0/3          Status: ESMC Tx (QL PRC/SSM 0x2)
6             Interface name: xe-0/0/4          Status: ESMC Tx (QL PRC/SSM 0x2)
```

SyncE over LAG is supported only on MX Series. You should configure the member interface as the SyncE source interface with the additional knob `aggregated-ether ae0` to enable SyncE functionality over LAG.

Configuring Squelching on BITS and Ethernet Interface

Refer to Figure 2.11 to understand the squelch functionality on SyncE. Also refer to the configuration on R1 of Ring1 in Example 2.19. In this case, R1 of Ring1 is providing clock to Ring2 via the xe-0/0/3 interface. In normal cases the output QL advertised by R1 is PRC. Now let's consider that the SyncE quality in Ring1 degraded from QL-PRC to QL-SSU or any other lower quality. But since the threshold QL for triggering squelch is configured as PRC (line number 33), and the output QL on R1 is degraded below the configured threshold, the output QL will be squelched. Since the supported squelch method is QL-DNU (line number 32), R1 will advertise QL-DNU towards Ring-2. On receiving QL-DNU, R2 and the entire Ring-2 moves to holdover mode instead of tracking a degraded clock.

In case of BITS, the output squelching is enabled by line 16 in Example 2.19. Whenever the node output quality goes below the `minimum-quality`, the output will be squelched.

NOTE Squelching on Ethernet interface is supported only on the ACX710 platform. However, squelching support in BITS is supported on both the MX and ACX platforms.

Example 2.19 Configuration of Squelching on SyncE Interface on R1-Ring1

```
1       user@R1# show chassis synchronization
2       network-option option-1;
3       selection-mode received-quality;
4       quality-mode-enable;
5       clock-mode auto-select;
6       interfaces bits {
7           signal-type e1;
8           e1-options {
9               framing g704;
10          }
11      }
12      output {
13          interfaces bits {
14              wander-filter-disable;
15              source-mode chassis;
16              minimum-quality prc;
17          }
18      }
19      source {
20          interfaces xe-0/0/1 {
21              wait-to-restore 0;
22              quality-level prc;
23          }
24          interfaces xe-0/0/2 {
25              wait-to-restore 0;
26              quality-level prc;
27          }
28      }
29      esmc-transmit {
30          interfaces xe-0/0/3 {
31              squelch {
32                  method ql-dnu;
33                  quality-level prc;
34              }
35          }
36      }
```

The status of ESMC transmit details before and after squelching the output QL is represented in the following examples.

Example 2.20 ESMC Transmits detail on R0-Before Squelching

```
1       user@R1# run show synchronous-ethernet esmc transmit detail
2       ESMC Transmit interface details:
3           Interface name: xe-0/0/1          Status: ESMC Tx (QL DNU/SSM 0xf)
4           Interface name: xe-0/0/2          Status: ESMC Tx (QL PRC/SSM 0x2)
5           Interface name: xe-0/0/3          Status: ESMC Tx (QL PRC/SSM 0x2)
```

Example 2.21 ESMC Transmits detail on R0-After Squelching

```
1       user@R1# run show synchronous-ethernet esmc transmit detail
2       ESMC Transmit interface details:
3           Interface name: xe-0/0/1          Status: ESMC Tx (QL DNU/SSM 0xf)
4           Interface name: xe-0/0/2          Status: ESMC Tx (QL PRC/SSM 0x2)
5           Interface name: xe-0/0/3          Status: ESMC Tx (QL DNU/SSM 0xf)
```

Basic SyncE Troubleshooting Practices

Check all the basic SyncE configuration nuances on the router:

Make sure a PRC traceable clock source is used for feeding the clock to the network.

Make sure the configurations are correct. Refer to Chapter 2.

For XFP interface, make sure the framing mode LAN is configured under `chassis fpc <slot> pic <slot> framing lan'`.

For ESMC Tx/Rx, IFL or sub-interfaces must be configured under the IFD.

Know the limitations captured in the first chapter.

Enable and log all traces related to clock synchronization and verify these logs for any errors and anomalies:

```
user@R0# show protocols
clock-synchronization {
    traceoptions {
        file Clock size 1000000;
        flag all;
        flag debug;
    }
}
```

Check Synchronization Lock Status and verify the chassis is locked with no alarm/error:

```
user@R0# run show chassis synchronization extensive
Current clock status  : Locked
Clock locked to       : Primary
SNMP trap status      : Disabled

Configured interfaces:

Name         : external-0/0
Signal type  : 10mhz
Rx status    : disabled
Tx status    : active
LED color    : green

Configured outputs:

Interface      : external-0/0
Tx status      : active
Minimum QL     : SEC             Tx QL         : DNU
Holdover mode  : enabled         Wander filter : disabled
Source mode    : chassis         Source Tx DNU : disabled
Holdover data  : valid
Current state  : locked to chassis
  State for    : 9 days, 00 hrs, 29 mins, 06 secs
  State since  : Mon Aug 31 20:29:04 2020



Configured sources:
```

```
Interface           : xe-0/0/1
Status              : Primary       Index       : 257
Clock source state  : Clk qualified Priority    : Default(8)
Configured QL       : PRC           ESMC QL     : PRC
Clock source type   : ifd           Clock Event : Clock locked
Wait-to-restore     : 0  min        Hold-off    : 1000 ms
Interface State     : Up,pri,ESMC Rx(SSM 0x2),ESMC TX(QL DNU/SSM 0xf),
```

Check the chassis synchronization clock-module. This will indicate how long the clock module is in locked state:

```
user@R0# run show chassis synchronization clock-module
re0:

Clock module on SCB0
  Current role     : master
  Current state    : locked to external-0/0
    State for      : 8 days, 00 hrs, 15 mins, 17 secs
    State since    : Tue Sep  1 20:28:21 2020
  Monitored clock sources
    Interface      Type         Status
    external-0/0   e1           qualified-selected
```

Check that the ESMC is correctly received and transmitted by the configured interfaces:

```
user@R0# run show synchronous-ethernet esmc transmit detail
ESMC Transmit interface details:

    Interface name: xe-0/0/1          Status: ESMC Tx (QL DNU/SSM 0xf)
    Interface name: xe-0/0/2          Status: ESMC Tx (QL PRC/SSM 0x2)
    Interface name: xe-0/0/3          Status: ESMC Tx (QL PRC/SSM 0x2)
```

Check the ESMC statistics on the configured IFL. Make sure that the statistics are fine:

```
user@R0# run show synchronous-ethernet esmc statistics detail
ESMC Statistics:

Interface Name  :  xe-0/0/1
Transmit Count  :  480576            Receive Count        : 480860
Total Drop Count:  5                 Ineligible Drop Count: 0
Adjacency Count :  85

Interface Name  :  xe-0/0/2
Transmit Count  :  575108            Receive Count        : 574413
Total Drop Count:  0                 Ineligible Drop Count: 0
Adjacency Count :  4
```

Check the clock ref-info on the SyncE configured line card. This will indicate the status of chassis clock from CB0 and CB1 (Ref4 and Ref5):

```
RMPC1(R0 vty)# sh clksync ref-info
System mode : Centralized
   SCB0 Ref - Ref id 4
      SCM status   : Good
      CFM status   : Good
      GST status   : Good
      PFM status   : Good
   SCB1 Ref - Ref id 5
      SCM status   : Good
      CFM status   : Good
```

```
      GST status    : Good
      PFM status    : Good

1 PPS reference not configured ...
   fsm state     : Init state
   Last event    : No clock
```

Check the clock DPLL info on the SyncE configured line card. This will indicate the status of DPLL-1 for Ref4 from CB0:

```
RMPC1(R0 vty)# sh clksync dpll-info
DPLL-1 Configuration ...
   Mode                  : Forced reference-lock
   Selected Reference    : 4
DPLL-1 Status....
   Lock Status       : Locked
   Lost Lock Status : False
   Holdover Status   : False
DPLL-2 Configuration ...
   Mode                  : Forced reference-lock
   Selected Reference    : 7
DPLL-2 Status....
   Lock Status       : Locked
   Lost Lock Status : False
   Holdover Status   : False
DPLL-3 Configuration ...
   Mode                  : Forced reference-lock
   Selected Reference    : 2
DPLL-3 Status....
   Lock Status       : Unlocked
   Lost Lock Status : False
   Holdover Status   : False
DPLL-4 Configuration ...
   Mode                  : Forced reference-lock
   Selected Reference    : 0
DPLL-4 Status....
   Lock Status       : Unlocked
   Lost Lock Status : False
   Holdover Status   : False
```

Synchronous Ethernet Support on Juniper Platforms

As of the writing of this book, Synchronous Ethernet as per ITU-T G.8262, is supported on the following platforms/line cards:

- Juniper MX series of router support Synchronous Ethernet starting MPCEX (X=1 to 11), NG-MPCE2/3, MX80-T/P, MX104, MX204, MX10003, and MX10K-LC2101.
- Juniper ACX series of router support Synchronous Ethernet on the following platforms: ACX500, ACX1000, ACX1100, ACX2100, ACX2200, ACX4000, ACX5448, ACX5448-D, ACX5448-M, ACX710, ACX7100-32C, and ACX7100-48L.
- Juniper PTX series of routers PTX3000 and PTX5000 support Synchronous Ethernet Feature.

NOTE The MX Series platform uses SCBE and supports centralized clocking mode from 12.2 release onward. With SCBE2, centralized mode is

supported from Junos release 13.3 onward.

NOTE The MX Series of line cards starting MPCEX (X=7 to 10), MX204, and MX10003 have hardware capability for Enhanced Synchronous Ethernet as per ITU-T G.8262.1.

Summary

This chapter discussed Synchronous Ethernet technology in detail, with ESMC packets and the associated QL values. The clock selection algorithm selects the best clock from the available candidate clocks and advertises the selected clock in the downstream direction based on configuration options such as quality mode, selection mode, received quality, and configured quality. It discussed the Junos configurations for clock propagation across a linear chain of nodes, ring topologies, and various failure conditions. It also discussed basic troubleshooting practices. SyncE can also be configured over aggregated Ethernet. Various Juniper platforms and line cards that support SyncE are covered last.

Chapter 3

Precision Time Protocol

NOTE While publishing this book, the IEEE1588v2 standard bodies had not yet converged on a *Master/Slave* terminology alternative, so this book uses *Master/Client* instead of *Master/Slave* in descriptive text and figures, leaving "slave" in code and output. As soon as the standards bodies agree, this notice will disappear and the book will be updated throughout with agreed upon terms, including new Junos CLI.

What is PTP?

The Precision Time Protocol (PTP), also known as *1588v2* in the telecom world, is an IEEE standard protocol that enables precise transfer of frequency and time over packet-switched Ethernet networks. It synchronizes the local clock on the device, usually known as a client clock, with reference to a master clock, known as a grandmaster clock, and delivers a high level of synchronization accuracy, in both phase and frequency. The high precision is made possible with the help of PHY/MAC timestamping for the PTP packets that are exchanged between the master and client clock.

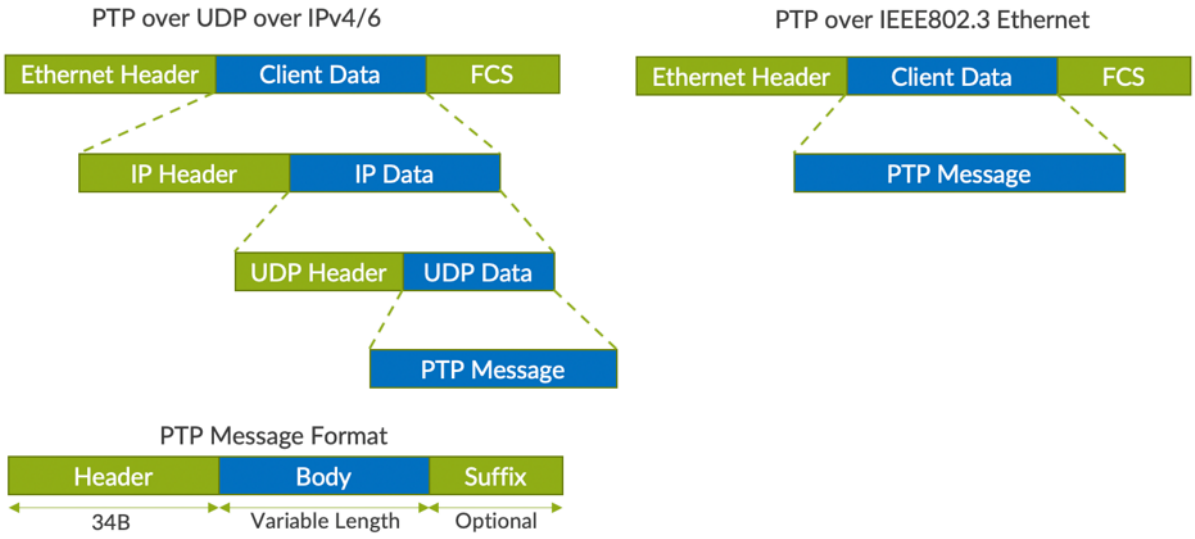
PTP Packet Format

PTP messages can be transported over several types of protocols. The most important of them are:

- PTP over UDP over IPV4
- PTP over UDP over IPv6
- PTP over IEEE802.3 Ethernet

Figure 3.1 illustrates the encapsulation of PTP messages over lower layer protocols. For more details on the PTP packet decodes refer to the Appendix of this book.

Figure 3.1 PTP Packet Format



PTP Clock Types

PTP clocks are mainly classified into four types:

- Ordinary Clock
- Boundary Clock
- End-to-End Transparent Clock
- Peer-to-Peer Transparent Clock

The *Ordinary clock* can be either Ordinary Master or Ordinary Client. The Ordinary Master is also referred as the Grand Master. The Grand Master clock uses GPS input to deliver PTP.

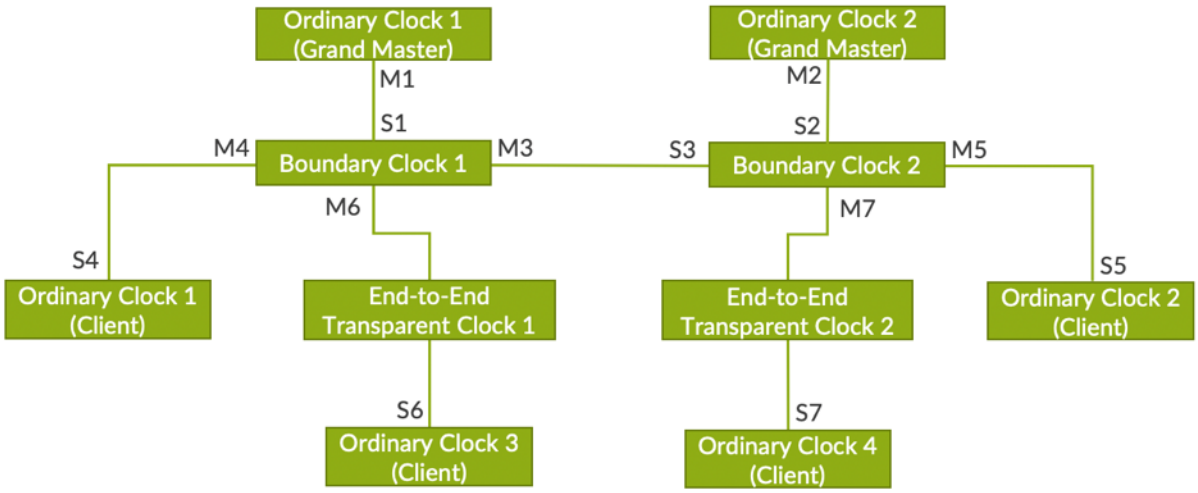
The *Boundary clock* is usually a multi-port device that can act as master and client clock. The Client can recover the clock from the upstream master and the master can distribute the clock to downstream client.

The *End-to-End Transparent Clock* is neither a master nor a client. It forwards the packet and accounts for the packet residence time within the device. This helps the downstream client estimate and remove the variable delay experienced by the Transparent Clock.

The *Peer-to-Peer Transparent Clock* is similar to the End-to-End Transparent Clock. It forwards sync and follow-up messages only to account for the residence time. A correction field includes the sum of residence delay and peer-to-peer link delay.

Figure 3.2 depicts the various PTP clock types.

Figure 3.2 PTP Clock Types



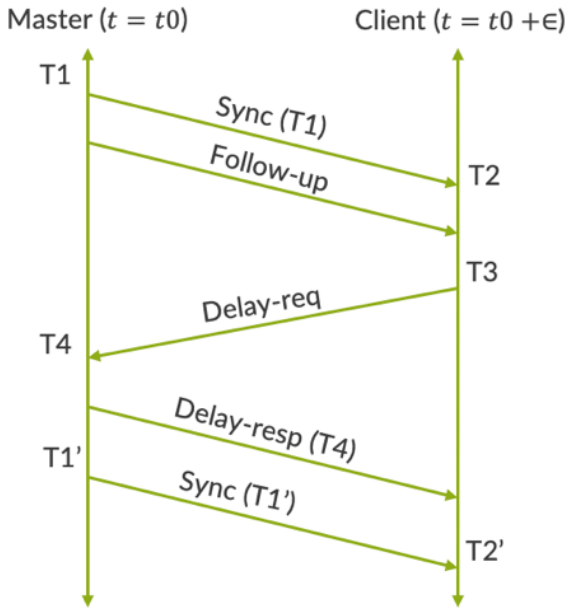
PTP Clock Synchronization

In the IEEE 1588 system, all clocks are organized into a master-client hierarchy. The master and client exchanges certain messages to synchronize client time with master time. There are five message types defined by PTP:

- Sync
- Delay-request
- Follow-up
- Delay-response
- Management

The message types sync and delay-req are called “event messages,” since they are used as timing events by the PTP protocol. Message types follow-up, delay-resp, and management are called “general messages.” The rates of these PTP messages are profile specific, which we will see in the upcoming Profile section.

Figure 3.3 PTP Clock Synchronization



Let's discuss how we can synchronize two clocks over a packet network. Consider two clocks, say Clock1 and Clock2 as shown in Figure 3.3, and let's assume Clock1 is the master and Clock2 is the client. There could be some offset at the beginning between these two clocks. Let this offset be ∈'. As time progresses, this offset might change, which means there is frequency drift. However, for all practical purposes, let's assume that the frequency drift is very small for the duration of the message exchange interval. In other words, both master and client are equipped with stable oscillators.

Let's understand the messages exchange between master and client. Initially the master sends out sync message towards the client that contain the approximate timestamp for the time-of-departure, T1 of the sync message based on the master's own clock. The client records the arrival time of the sync message via the timestamp T2 according to the client's own clock. Now, the client sends Delay_Req message to the master and T3 is the time of departure of the delay-request message as recorded by the client. The master records the arrival time of the Delay_Req message as T4 and communicates T4 to the client by sending a Delay_Resp message.

Let's say the time taken for the sync message to travel from master to client is Δ_{ms} and the time taken for the Delay_Req message to travel from client to the master is Δ_{sm}. With this we can arrive at the two mathematical equations below:

$$Forward\ Delay\ '\Delta_{ms}' = T1 - (T2+\epsilon)$$

$$Reverse\ Delay\ '\Delta_{sm}' = (T3+\epsilon) - T4$$

So we now have two equations and three variables. To solve these equations, we need to make one assumption that the forward delay is same as the reverse delay.

$$\Delta = \Delta_{ms} = \Delta_{sm}\ (Assumption)$$

Now one can solve the above two equations to compute the initial offset ′ ∈ ′ and delay ′Δ′ and the client can synchronize with the master time by compensating these offsets and delays.

$$\in = \frac{(T2 - T1) - (T4 - T3)}{2}$$

$$\Delta = \Delta_{ms} = \Delta_{sm} = \frac{(T2 - T1) + (T4 - T3)}{2}$$

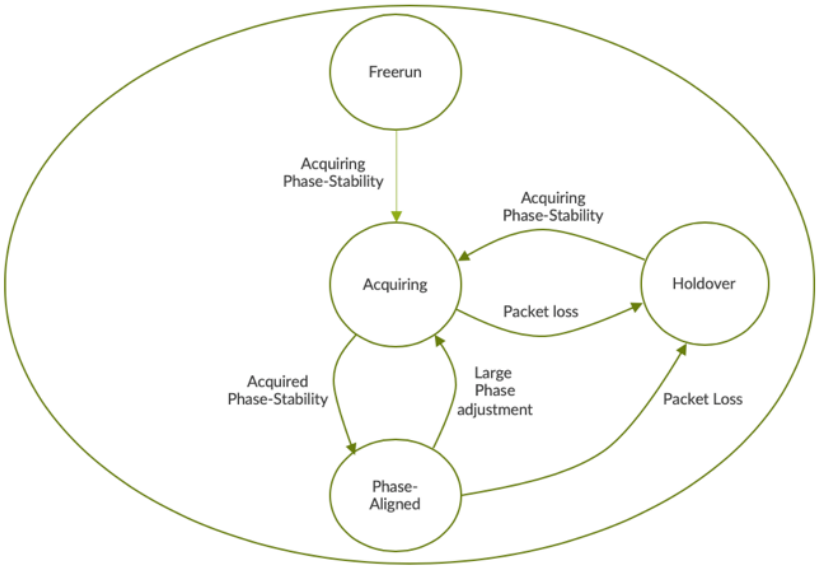
In reality, this process continues periodically for streams of packets between master and client, to obtain the best estimate of the client's time with respect to that of the master. Since we have made a big assumption, that forward delay is same as reverse delay, the actual difference in these delays leads to the error in the estimation of clock offset. So the effect of path asymmetry on the calculation of clock offset can lead to an error in the offset computation, and this error amounts to half of the asymmetry in the assumed delays.

$$Error\ in\ Offset = \frac{(Forward\ Delay - Reverse\ Delay)}{2}$$

PTP Local Clock-State Machine

The state machine in Figure 3.4 represents the local clock synchronization state during various conditions.

Figure 3.4 PTP Local Clock State Machine



In Figure 3.4 the local clock delivers the PTP clock with TOD and frequency synchronized to the grandmaster clock. It is comprised of a servo and clock module. Once the timing signals arrive at the servo, it estimates the time offset of the PTP clock and adjusts the frequency and time of the clock module in an attempt to maintain the estimated offset within acceptable tolerances. Free-run is the default state of the local clock, when the device is not connected to any external source with PTP, configuration is enabled.

As soon as the local clock receives PTP packets from the upstream device, it changes its state from free-run to acquiring. The state of the local clock is a function of the servo control algorithm to find a consistent PDV baseline, often referred to as *the minimum floor*. The PTP servo algorithm takes samples of packets within a chosen time window specific to the profiles or applications, and finds a stable packet delay floor. Once this is being identified and filtered, the oscillator is adjusted to align the frequency/phase with the reference clock or grandmaster clock with some level of error margin or variation. The state of the local clock in this state is represented as Phase-Aligned.

It is important to note that the margin of offset/error and the duration for which the clock remains in acquiring states before moving to phase-aligned state are dependent on the packet delay variation magnitude, duration, type, and the stability of the recovered frequency. With hybrid mode, as we have a stable physical layer frequency, the local clock state will quickly move to phase-aligned state. Even in the phase-aligned state, if the magnitude of PDV is increased beyond a certain value or if the floor delay is shifting continuously, then local clock state changes back to acquiring state and it may continue in this state for a sufficiently long time until the servo control algorithm is able to correct it. In certain cases, if the local clock fails to receive PTP packets from its upstream, the state changes to holdover from acquiring/phase-aligned state. The output phase in this case is delivered using the acquired holdover history. Holdover state changes to acquiring state when the local clock starts receiving packets from the upstream master.

Clock Selection Algorithms

Clock Selection Algorithms (CSA), commonly known as Best Master Clock Algorithm (BMCA) in 1588 parlance, is primarily used to elect the best master clock from the pool of available master clocks for use by the given client clock. It consists of two parts. The first part is a state decision algorithm (SDA) and the second part is the data set comparison algorithm

(DCA). The later compares the data sets of two or more masters for use by a given client clock and determine its best master. The state decision algorithm however decides the recommended states as per PTP state machine defined in the IEEE 1588-2008 standard. The recommended port state can be listening, master, client, or passive. Refer to the 1588v2 and ITU-T standards for more details.

What Are PTP Profiles?

PTP profiles enable the specific selection of PTP attribute values and features to facilitate interwork with other PTP devices and provide performance that meets the requirements of particular applications. There are a number of PTP profiles:

- IEEE Telecom Profile 2008 (1588v2 Profile)
- ITU-T PTP Telecom Profile for Frequency (G.8265.1 Profile)
- ITU-T PTP Telecom Profile for Phase/Time (G.8275.1 Profile)
- ITU-T PTP Telecom Profile for Phase/Time (G.8275.2 Profile)
- IETF Enterprise Profile
- Media Profile
  - SMPTE ST-2059-2
  - AES67
  - AES67+SMPTE ST-2059-2

NOTE The Juniper MX Series of devices supports a proprietary enhanced version of G.8275.1 profile. This is known as G.8275.1.enh Profile. This profile enables both PTP over IPv4 and PTP over Ethernet transport with added support on single/dual tagged VLANs. G.8275.1.enh profile with PTP over IPv4 transport currently doesn't support unicast negotiation.

NOTE At the time of the writing of this book, only the MX Series of devices and the ACX710 support the G.8275.1 phase profile. The G.8265.1 profile is not currently supported in any of the Junos platforms. Check for updates.

Let's look at the various attributes of these profiles. Tables 3.1 through 3.6 provide a quick summary of the configurable parameters that are very specific to each profile.

IEEE 1588-2008 Profile - Default Profile

IEEE 2008 defined the Default profile intend to address many common applications in various sectors other than industrial automation on PTP capable devices. In Junos it is referred as IEEE-2008 profile. This is the default profile on Junos platforms.

Table 3.1 IEEE 1588-2008 Profile

	IEEE	Juniper
Profile Name	**Default**	**IEEE-2008 (Note 1)**
Allowed Clock	**Ordinary Clock, Boundary Clock Transparent Clock**	**Ordinary Clock, Boundary Clock Transparent Clock**
Transport	**No restriction**	**IPv4, Ethernet**
Multicast or Unicast	**All messages are sent in Unicast.**	**Unicast for PTP over IPv4 Multicast for PTP over Ethernet**
Unicast Negotiation	**Default**	**Not enabled by default**
BMCA	**Default**	**Default**
VLAN	**Supported**	**Supported**
Sync & Follow-up	**Range: 2^1 *to* 2^{-7} Default: 2^{-4}**	**Range: 2^7 *to* 2^{-7} for master (Note 2) Default: 2^{-6} for client, 2^{-7} for master (Note 2)**
Delay-Req & Delay-Resp	**Range: 2^6 *to* 2^{-7} Default: 2^{-4}**	**Range: 2^7 *to* 2^{-7} (Note 2) Default: 2^{-4} for client, 2^{-7} for master (Note 2)**
Announce	**Range: 2^3 *to* 2^{-3} Default: 2^1**	**Range: 2^4 *to* 2^{-3} (Note 3) Default: 2^1 for client, 2^{-3} for master (Note 3)**
Signaling	**As per Unicast Negotiation**	**As per Unicast Negotiation**
Priority1	**Range: 0 *to* 255 Default: 128**	**Range: 0 *to* 255 Default: 128**
Priority2	**Range: 0 *to* 255 Default: 128**	**Range: 0 *to* 255 Default: 128**
Domain Number	**Range: 0 *to* 127 Default: 0**	**Range: 0 *to* 127 Default: 0**
Local Priority	**Not Applicable**	**Not Applicable**
maxStepsRemoved	**Not Applicable**	**Not Applicable**
Announce Receipt Time-out	**Range: 2 *to* 10 Default: 3**	**Range: 2 *to* 10 Default: 3**
Duration Field	**Range: 10 *to* 1000 Default: 300**	**Range: 60 *to* 1000 Default: 300**
MasterOnly	**Not Applicable**	**Supported**
SF	**Not Applicable**	**Not Applicable**
Packet Timing Signal Fail	**Not Applicable**	**Not Applicable**

Note 1: This is the default profile. When a profile is not configured, then the device uses default profile.

Note 2: The value mentioned in this table is for the MX platform. For the ACX platform, the default value of Sync and Delay-Req is -6 for both Client and Master. Configurable range for Sync and Delay-Req is -3 to -6 for Client and 4 to -7 for Master.

Note 3: The value mentioned in table is for MX platform. For ACX platform, the default value of Announce is 1 for Master. Configurable range for Announce is 0 to 3 for Master.

ITU-T PTP Telecom Profile for Phase/Time - G.8275.1 Profile

The G.8275.1 profile is also called Phase-profile for on-path support. This profile requires all devices in the network to operate in combined or hybrid modes, which means PTP and SyncE enabled on all devices. The G.8275.1 profile is defined for PTP over multicast Ethernet Transport.

Table 3.2 ITU-T g.8275.1 Profile

	ITU-T	Juniper
Profile Name	**g.8275.1**	**g.8275.1**
Allowed Clock	**Ordinary Clock, Boundary Clock** **End-to-End Transparent Clock**	**Ordinary Clock** **Boundary Clock (Note-1)**
Transport	**IEEE802.3 Ethernet**	**IEEE802.3 Ethernet**
Multicast or Unicast	**Multicast**	**Multicast**
Unicast Negotiation	**Not Applicable**	**Not Applicable**
BMCA	**Alternate BMCA**	**Alternate BMCA**
VLAN	**Not supported**	**Not supported**
Sync & Follow-up	**Range: 2^{-4} ($16PPS$)** **Default: 2^{-4} ($16PPS$)**	**Range: 2^{-4}(16PPS)** **Default: 2^{-4}(16PPS)**
Delay-Req & Delay-Resp	**Range: 2^{-4} (16PPS)** **Default: 2^{-4}(16PPS)**	**Range: 2^{-4}(16PPS)** **Default: 2^{-4}(16PPS)**
Announce	**Range: 2^{-3}(8PPS)** **Default: 2^{-3}(8PPS)**	**Range: 2^{-3}(8PPS)** **Default: 2^{-3}(8PPS)**
Signaling	**Not Applicable**	**Not Applicable**
Priority1	**Range: 128** **Default: 128**	**Range: 128** **Default: 128**
Priority2	**Range: 0 *to* 255** **Default: 128**	**Range: 0 *to* 255** **Default: 128**
Domain Number	**Range: 24 *to* 43** **Default: 24**	**Range: 24 *to* 43** **Default: 24**
Local Priority	**Range: 1 *to* 255** **Default: 128**	**Range: 1 *to* 255** **Default: 128**
maxStepsRemoved	**Range: 1 *to* 255** **Default: 255**	**Not Supported**
Announce Receipt Time-out	**Range: 2 *to* 10** **Default: 3**	**Range: 2 *to* 10** **Default: 3**
Duration Field	**Not Applicable**	**Not Applicable**
MasterOnly	**Supported**	**Supported**
SF	**Not Applicable**	**Not Applicable**
Packet Timing Signal Fail	**Not Applicable**	**Not Applicable**

Note 1: ACX710 platform supports virtual-port configuration with T-BC, which shall enable Assisted Full Timing Support & GM functionality.

G.8275.1.enh profile for Phase/Time

Juniper has introduced a profile for phase/time. This is referred to as G.8275.1.enh profile, an enhanced version of G.8275.1 with added support that enables PTP over IPv4 and additional VLAN configurations.

Table 3.3 ITU-T g.8275.1.enh Profile

	ITU-T	Juniper
Profile Name		**G.8275.1.enh (Note 1)**
Allowed Clock		**Ordinary Clock, Boundary Clock**
Transport		**IPv4, Ethernet**
Multicast or Unicast		**Unicast for PTPoIPv4** **Multicast for PTPoE**
Unicast Negotiation		**Not supported**
BMCA		**Alternate BMCA (Note 2)**
VLAN		**Supported**
Sync & Follow-up		**Range: 2^{7} *to* 2^{-7}** **Default: 2^{-4}**
Delay-Req & Delay-Resp	**Not Applicable**	**Range: 2^{6} *to* 2^{-7}** **Default: 2^{-4}**
Announce		**Range: 2^{4} *to* 2^{-3}** **Default: 2^{-3}**
Signaling		**Not supported**
Priority1		**Range: 128** **Default: 128**
Priority2		**Range: 0 *to* 255** **Default: 128**
Domain Number		**Range: 0 *to* 127** **Default: 24**
Local Priority		**Range: 1 *to* 255** **Default: 128**
maxStepsRemoved		**Not Supported**
Announce Receipt Time-out		**Range: 2 *to* 10** **Default: 3**
Duration Field		**Not applicable**
MasterOnly		**Supported**
SF		**Not Applicable**
Packet Timing Signal Fail		**Not Applicable**

ITU-T PTP Telecom Profile for Phase/Time – G.8275.2 Profile

The G.8275.2 profile is a telecom profile for phase/time synchronization with Partial Timing Support (PTS) or Assisted Partial Timing Support (APTS) from the network. This profile therefore introduces Telecom Boundary Clock for Partial Timing Support (T-BC-P) and Telecom Boundary Clock for Assisted Partial Timing Support (T-BC-A). Similarly, T-TSC-P and T-TSC-A for Telecom Time Client Clock for Partial and Assisted Partial Timing Support, respectively. T-BC-P uses PTP input as the primary source of synchronization, whereas T-BC-A uses PTP as a secondary source of synchronization to hold the time for up to 72 hours in the event of GNSS outage, which is the primary source.

Table 3.4 ITU-T g.8275.2 Profile

	ITU-T	Juniper
Profile Name	**g.8275.2**	**g.8275.2.enh (Note 1)**
Allowed Clock	**Ordinary Clock, Boundary Clock** **Transparent Clock is for further study.**	**Ordinary Clock** **Boundary Clock**
Transport	**IPv4, IPv6**	**IPv4, IPv6**
Multicast or Unicast	**Unicast for PTPoIPv4 and PTPoIPv6**	**Unicast for PTPoIPv4 and PTPoIPv6**
Unicast Negotiation	**Mandatory**	**Not Mandatory (Note 2)**
BMCA	**Alternate BMCA**	**Alternate BMCA**
Sync & Follow-up	**Range: 2^0 *to* 2^{-7}** **Default: No default specified**	**Range: 2^0 *to* 2^{-7}** **Default: 2^{-6} *for client and* 2^{-7} *for master***
Delay-Req & Delay-Resp	**Range: 2^0 *to* 2^{-7}** **Default: No default specified**	**Range: 2^0 *to* 2^{-7}** **Default: 2^{-6} *for client and* 2^{-7} *for master***
Announce	**Range: 2^0 *to* 2^{-3}** **Default: No default specified**	**Range: 2^0 *to* 2^{-3}** **Default: 2^0 *for slave and* 2^{-3} *for master***
Signaling	**As per Unicast Negotiation**	**As per Unicast Negotiation**
Priority1	**Range: *Not used*** **Default: 128**	**Range: *Not used*** **Default: 128**
Priority2	**Range: 0 *to* 255** **Default: 128**	**Range: 0 *to* 255** **Default: 128 *for* T-BC** **Default: 255 *for* T-TSC-P and T-TSC-A**
Domain Number	**Range: 44 *to* 63** **Default: 44**	**Range: 44 *to* 63** **Default: 44**
Local Priority	**Range: 1 *to* 255** **Default: 128**	**Range: 1 *to* 255** **Default: 128**
Announce Receipt Time-out	**Range: 2 *to* 10**	**Range: 2 *to* 10** **Default: 3**

	Default: 2 (2 missing Announce message)	
Duration Field	**Range: 60 *to* 1000** **Default: 300**	**Range: 60 *to* 1000** **Default: 300**
MasterOnly	**Supported**	**Supported**
SF	**TRUE when the client port is in Signal Failure**	**Not supported**
Packet Timing Signal Fail	**PTSF-lossSync** **PTSF-unusable**	**Not supported**

Note 1: On the ACX5448 and QFX platforms, the profile is named as G.8275.2.enh. However, on ACX710 the profile is named as G.8275.2.

Note 2: Unicast Negotiation is disabled by default on ACX5448 and QFX platform. A user can enable it by using explicit command. However, on ACX710, it is always enabled.

IETF Enterprise Profile for Phase/Time

IETF has developed the Enterprise Profile for Phase/Time, mainly intended for enterprise networks and financial markets such as High Frequency Trading (HFT), financial regulatory requirements, etc. It provides the ability for enterprise and financial markets to timestamp on different systems and to handle a range of latency and delays.

Table 3.5 IETF Enterprise Profile

	IETF	Juniper
Profile Name	**Default**	**Enterprise**
Allowed Clock	**Ordinary Clock, Boundary Clock**	**Ordinary Clock, Boundary Clock**
Transport	**No restriction**	**IPv4**
Multicast or Unicast	**All messages are sent in Unicast.**	**Multicast for PTPoIPv4**
Unicast Negotiation	**Not applicable**	**Not applicable**
BMCA	**Default**	**Default**
Sync & Follow-up	**Range: 2^{1}*to* 2^{-7}** **Default: 2^{-4}**	**Range: 2^{7}*to* 2^{-7}** **Default: 2^{0}**
Delay-Req & Delay-Resp	**Range: 2^{1}*to* 2^{-7}** **Default: 2^{-4}**	**Range: 2^{7}*to* 2^{-7}** **Default: 2^{0}**
Announce	**Range: 2^{3}*to* 2^{-3}** **Default: 2^{1}**	**Range: *Unsupported*** **Default: 2^{0}**
Signaling	**As per Unicast Negotiation**	**Not supported**
Priority1	**Range: 0 *to* 255** **Default: 128**	**Range: 0 *to* 255** **Default: 128**
Priority2	**Range: 0 *to* 255** **Default: 128**	**Range: 0 *to* 255** **Default: 128**
Domain Number	**Range: 0 *to* 127** **Default: 0**	**Range: 0 *to* 127** **Default: 0**

Announce Receipt Time-out	**Range: 2 *to* 10** **Default: 3**	**Range: 2 *to* 10** **Default: 3 *for preferred masters*** **4 *for other masters***
Duration Field	**Not applicable**	**Not applicable**
Packet Timing Signal Fail	**Not Applicable**	**Not Applicable**

Media Profile for Phase/Time

Media profile is defined to meet the IP audio/video broadcast network applications. These profiles help alignment of audio and video signals over IP links. This includes three PTP profiles: SMPTE ST 2059-1, AES67, and AES67+SMPTE ST-2059-2.

The SMPTE ST-2059-2 standard supports video applications for capture, video edit, and playback to be used in professional broadcast environments. The standard allows multiple video sources to stay in sync across various equipment by providing time and frequency synchronization to all devices.

AES67 supports professional quality audio applications for high performance streaming over IPv4 multicast transport in media networks with low latencies. It allows audio streams to be combined at a receiver, maintaining stream synchronization.

And AES67+SMPTE ST-2059-2 merges two standards with a common agreement for support and default values. It allows the interoperation of the two standards over the same network, so that common PTP assumptions can be used.

Table 3.6 SMPTE ST-2059-2 Media Profile

	SMPTE	Juniper
Profile Name	**SMPTE ST-2059-2**	**smpte**
Allowed Clock	**Ordinary Clock, Boundary Clock**	**Ordinary Clock, Boundary Clock**
Transport	**IPv4, IPv6, IGMPv2**	**IPv4, IGMPv2**
Multicast or Unicast	**Multicast for IPv4 and IPv6**	**Multicast for PTP over IPv4**
Unicast Negotiation	**NA**	**NA**
BMCA	**Default**	**Default**
Sync & Follow-up	**Range: 2^{-1}*to* 2^{-7}** **Default: 2^{-3}**	**Range: 2^{-1}*to* 2^{-7}** **Default: 2^{-3}**
Delay-Req & Delay-Resp	**portDS.logSyncInterval+5**	**Range: 2^{-3}*to* 2^{-7}** **Default: 2^{-3}**
Announce	**Range: 2^{1}*to* 2^{-3}**	**Range: 2^{1}*to* 2^{-3}**

	Default: 2^{-2}	**Default: 2^{-2}**
Signaling	**As per Unicast Negotiation**	**As per Unicast Negotiation**
Priority1	**Range: 0 *to* 255** **Default: 128**	**Range: 0 *to* 255** **Default: 128**
Priority2	**Range: 0 *to* 255** **Default: 128**	**Range: 0 *to* 255** **Default: 128**
Domain Number	**Range: 0 *to* 127** **Default: 127**	**Range: 0 *to* 127** **Default: 127**
Announce Receipt Time-out	**Range: 2 *to* 10** **Default: 3**	**Range: 2 *to* 10** **Default: 3**
Delay-request Time-out	**Range: 30 *to* 300** **Default: 30**	**Range: 30 *to* 300** **Default: 30**
Duration Field	**Not applicable**	**Not applicable**
Packet Timing Signal Fail	**Not Applicable**	**Not Applicable**

Table 3.7 AES Media Profile

	SMPTE	Juniper
Profile Name	**aes67**	**aes67**
Allowed Clock	**Ordinary Clock, Boundary Clock**	**Ordinary Clock, Boundary Clock**
Transport	**IPv4, IPv6, IGMPv2**	**IPv4, IGMPv2**
Multicast or Unicast	**Multicast for IPv4 and IPv6**	**Multicast for PTP over IPv4**
Unicast Negotiation	**NA**	**NA**
BMCA	**Default**	**Default**
Sync & Follow-up	**Range: 2^{1}*to* 2^{-4}** **Default: 2^{-3}**	**Range: 2^{1}*to* 2^{-4}** **Default: 2^{-3}**
Delay-Req & Delay-Resp	**Range: 2^{5}*to* 2^{-3}** **Default: 2^{0}** **(portDS.logSyncInterval to portDS.logSyncInterval+5)**	**Range: 2^{-3}*to* 2^{-7}** **Default: 2^{-3}**
Announce	**Range: 2^{4}*to* 2^{0}** **Default: 2^{1}**	**Range: 2^{4}*to* 2^{0}** **Default: 2^{1}**
Signaling	**As per Unicast Negotiation**	**As per Unicast Negotiation**
Priority1	**Range: 0 *to* 255** **Default: 128**	**Range: 0 *to* 255** **Default: 128**
Priority2	**Range: 0 *to* 255** **Default: 128**	**Range: 0 *to* 255** **Default: 128**
Domain Number	**Range: 0 *to* 255** **Default: 0**	**Range: 0 *to* 255** **Default: 0**
Announce Receipt Time-out	**Range: 2 *to* 10** **Default: 3**	**Range: 2 *to* 10** **Default: 3**
Delay-request Time-out	**Range: 30 *to* 300** **Default: 30**	**Range: 30 *to* 300** **Default: 30**

Duration Field	**Not applicable**	**Not applicable**
Packet Timing Signal Fail	**Not Applicable**	**Not Applicable**

Table 3.8 AES+SMPTE ST-2059-2 Media Profile

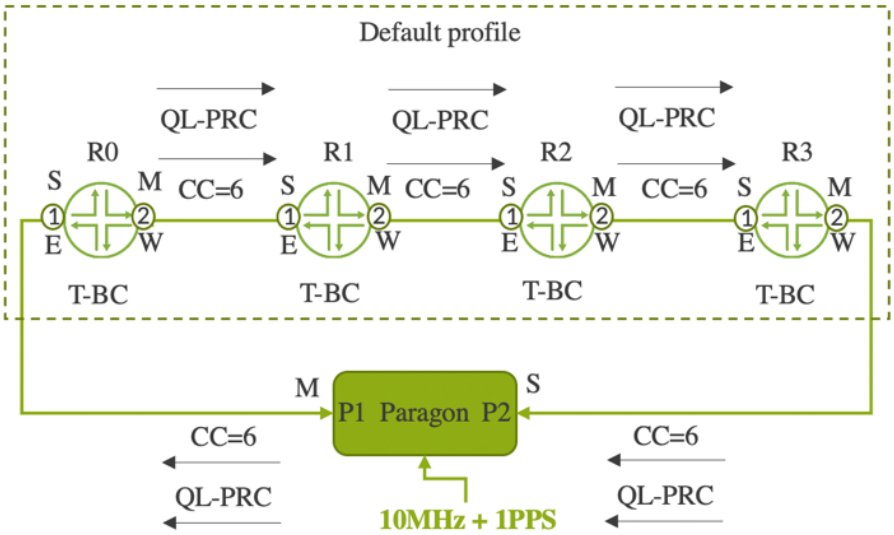
	SMPTE	Juniper
Profile Name	**AES67+SMPTE ST-2059-2**	**aes67+smpte**
Allowed Clock	**Ordinary Clock, Boundary Clock**	**Ordinary Clock, Boundary Clock**
Transport	**IPv4, IPv6, IGMPv2**	**IPv4, IGMPv2**
Multicast or Unicast	**Multicast for IPv4 and IPv6**	**Multicast for PTP over IPv4**
Unicast Negotiation	**NA**	**NA**
BMCA	**Default**	**Default**
Sync & Follow-up	**Range: 2^{-1}*to* 2^{-4}** **Default: 2^{-3}**	**Range: 2^{-1}*to* 2^{-4}** **Default: 2^{-3}**
Delay-Req & Delay-Resp	**Range: 2^{5}*to* 2^{-3}** **Default: 2^{0}** **(portDS.logSyncInterval to portDS.logSyncInterval+5)**	**Range: 2^{-3}*to* 2^{-7}** **Default: 2^{-3}**
Announce	**Range: 2^{1}*to* 2^{0}** **Default: 2^{0}**	**Range: 2^{1}*to* 2^{0}** **Default: 2^{0}**
Signaling	**As per Unicast Negotiation**	**As per Unicast Negotiation**
Priority1	**Range: 0 *to* 255** **Default: 128**	**Range: 0 *to* 255** **Default: 128**
Priority2	**Range: 0 *to* 255** **Default: 128**	**Range: 0 *to* 255** **Default: 128**
Domain Number	**Range: 0 *to* 127** **Default: 0**	**Range: 0 *to* 127** **Default: 0**
Announce Receipt Time-out	**Range: 2 *to* 10** **Default: 3**	**Range: 2 *to* 10** **Default: 3**
Delay-request Time-out	**Range: 30 *to* 300** **Default: 30**	**Range: 30 *to* 300** **Default: 30**
Duration Field	**Not applicable**	**Not applicable**
Packet Timing Signal Fail	**Not Applicable**	**Not Applicable**

Configuring and Verifying PTP

Chain of T-BCs with default-profile

The network below is a chain of four T-BCs connected in linear fashion. The tester is operating in master/client emulation mode so that port P1 act as master and P2 as client. The tester requires a 1 pulse per second (1pps) and 10MHz reference clock from an external stratum1 clock source such as a Global Positioning System (GPS) or Rubidium (Rb) source.

Figure 3.5 Linear Chain of T-BCs with Default Profile



In Figure 3.5, the tester P1 provides both the PTP and SyncE clock to R0. R0 recovers the clock and locks in phase and frequency to the upstream master port P1. Accuracy of the end-to-end system can be improved by enabling the hardware to timestamp the PTP packets (see line 3 in Example 3.1), which will remove the PDV associated with the queuing system in the packet processing path. You can further improve the accuracy by configuring SyncE to stabilize the frequency at each node along with PTP. This combined mode of operation is called *hybrid mode* (see lines 11-14) and the network that supports this mode is said to operate in Full Timing Support (FTS). The configuration required in this case is furnished in Example 3.1. In this case, PTP over IPv4 transport is configured with the default profile (you need not explicitly configure any profile for default mode).

Example 3.1 Configuration of PTP on R0

```
user@R0# show protocols ptp
clock-mode boundary;
phy-timestamping;
slave {
    interface xe-0/0/1.0 {
        unicast-mode {
            transport ipv4;
            clock-source 100.0.0.1 local-ip-address 100.0.0.2;
        }
    }
    hybrid {
        synchronous-ethernet-mapping {
            clock-source 100.0.0.1 {
                interface xe-0/0/1;
            }
        }
    }
}
master {
    interface xe-0/0/2.0 {
        unicast-mode {
            transport ipv4;
            clock-client 101.0.0.1/32 local-ip-address 101.0.0.2;
        }
    }
}
```

Example 3.2 Configuration of chassis synchronization on R0

```
user@R0# show chassis synchronization
network-option option-1;
selection-mode received-quality;
quality-mode-enable;
source {
    interfaces xe-0/0/1 {
        wait-to-restore 0;
        quality-level prc;
    }
}
esmc-transmit {
    interfaces all;
}
```

Let's verify that these configurations are applied on R0, by running the CLI command in Example 3.3 to see if the R0 device is locked to its upstream frequency and PTP source. It is clear from the example that the PTP lock status is `phase-aligned` with a phase offset of 1 ns and the client interface is the interface connected to the upstream master, in this case tester port P1. The phase offset mentioned here is not an absolute measurement but a relative measurement on the average offset that is being computed in the phase aligned state based on the assumption of symmetrical delays between master and client. It is a relative measurement based on the PTP timestamps but cannot be used directly to compare with the tester since the tester has the master 1pps as a reference.

Example 3.3 Output of PTP lock status on R0

```
user@R0# run show ptp lock-status detail
Lock Status:

Lock State    : 5 (PHASE ALIGNED)
Phase offset  : 0.000000001 sec
State since   : 2020-06-24 03:32:06 PDT (1w5d 08:11 ago)

Selected Master Details:
Upstream Master address    : 00:00:00:00:00:00:00:01
Slave interface            : xe-0/0/1.0
Clock reference state      : Clock locked
1pps reference state       : Clock qualified
```

You can see that the `Upstream Master address 00:00:00:00:00:00:00:01` is the clock ID of the upstream master, port 1 of the tester. Let's now check the frequency lock status by running the following CLI command in Example 3.4. It's evident that the clock is locked to the primary source interface xe-0/0/1 and the `Current lock status` is `Locked`.

Example 3.4 Output of chassis synchronization status on R0

```
user@R0# run show chassis synchronization extensive
Current clock status  : Locked
Clock locked to       : Primary
SNMP trap status      : Disabled

Configured sources:

Interface           : xe-0/0/1
Status              : Primary       Index       : 312
Clock source state  : Clk qualified Priority    : Default(8)
Configured QL       : PRC           ESMC QL     : PRC
Clock source type   : ifd           Clock Event : Clock locked
Wait-to-restore     : 0  min        Hold-off    : 1000 ms
Interface State     : Up,pri,ESMC Rx(SSM 0x2),ESMC TX(QL DNU/SSM 0xf),
```

Since we have configured `hybrid mode`, it's good to verify the `hybrid status` using the following command in Example 3.5. This will indicate the lock status for frequency and phase in a single output.

Example 3.5 Output of hybrid status on R0

```
user@R0# run show ptp hybrid status
Hybrid Mode Status:
Configured Mode                : Hybrid
Operating  Mode                : Hybrid
PTP Reference                  : 00:00:00:00:00:00:00:01, xe-0/0/1.0
Synchronous Ethernet Reference : xe-0/0/1
Lock state                     : Locked
Lock state description         : Frequency Locked Phase Locked
```

The `Profile type, PHY Time Stamping` status, packet rates, and number of active client and master parameters can be seen in Example 3.6.

Example 3.6 Output of ptp global-information on R0

```
user@R0# run show ptp global-information
PTP Global Configuration:
Domain number           : 0
```

```
4         Clock mode              : Boundary
5         Profile type            : IEEE-2008
6         Priority Level1         : 128
7         Priority Level2         : 128
8         Local Priority          : <not applicable>
9         Path Trace              : Disabled
10        Unicast Negotiation     : Disabled
11        ESMC QL From Clock Class: Disabled
12        Clock Class/ESMC QL     :  -
13        SNMP Trap Status        : Disabled
14        PHY Time Stamping       : Enabled
15        UTC Leap Seconds        : 37
16        Transparent-clock-config : DISABLED
17        Transparent-clock-status : N/A
18        Slave Parameters:
19          Sync Interval         : <not applicable>
20          Delay Request Interval: -4 (16 packets per second)
21          Announce Interval     : <not applicable>
22          Announce Timeout      : 3
23          Grant Duration        : <not applicable>
24          Master Parameters:
25          Sync Interval               : -6 (64 packets per second)
26          Delay Request Interval      : <not applicable>
27          Announce Interval           : 1 (1 packet every 2 seconds)
28          Delay Request Timeout       : <not applicable>
29          Clock Step                  : one-step
30          Arbitrary Mode              : FALSE

31        Number of Slaves       : 1
32        Number of Masters      : 1
33        Number of Stateful     : 0
```

Now let's configure PTP over an Ethernet multicast transport with a default profile. Configuration of SyncE remains the same, so Example 3.7 does not repeat that.

Example 3.7 Configuration-PTP over Ethernet with default profile on R0

```
1         user@R0# show protocols ptp
2         clock-mode boundary;
3         phy-timestamping;
4         slave {
5             interface xe-0/0/1.0 {
6                 multicast-mode {
7                     transport {
8                         ieee-802.3;
9                     }
10                }
11            }
12            hybrid {
13                synchronous-ethernet-mapping {
14                    clock-source xe-0/0/1.0 {
15                        interface xe-0/0/1;
16                    }
17                }
18            }
19        }
20        master {
21            interface xe-0/0/2.0 {
22                multicast-mode {
23                    transport {
24                        ieee-802.3;
25                    }
26                }
27            }
28        }
```

Look at line numbers 5-8 and 20-24 in Example 3.7. You can see that both the client and master interface are configured in multicast-mode with the transport as ieee-802.3. Also, the IFL is configured as `clock-source` (line 14) whereas it is the upstream master IP address in the case of PTP over IPv4.

In both the PTP over IPv4 and the PTP over Ethernet case, with a default profile, all the devices R0-R3 are phase-aligned to the grandmaster clock (Tester port P1 in this case) via their upstream devices. All the clocks are using the Category-1 frequency source for the physical frequency reference from their upstream. Each node therefore advertises GM Clock Class 6 (CC=6) and QL=PRC to indicate the quality of the clock to its downstream node. Let's verify the clock output on each device as shown in Examples 3.8-3.11.

Example 3.8 Output of clock detail on R0

```
1       user@R0# run show ptp clock detail
2       Clock Details:

3       Slot Number           : 0
4       Default Data:
5       Two-step Clock        : FALSE          Clock Identity : 08:b2:58:ff:fe:e2:d7:d0
6       Total Ports on Device : 0                          Clock Class    : 248
7       Clock Accuracy        : 254                        Log Variance   : 15353
8       Clock Priority1       : 128                        Clock Priority2: 128
9       UTC Offset            : 37                         Leap59         : FALSE
10      Leap61                : FALSE                      Time Traceable : FALSE
11      Frequency Traceable   : FALSE                      Time Source    : 160
12      Delay Req Sending Time: 0                          Steps Removed  : 1
13      Slave-only            : FALSE
14      Parent Data:
15      Parent Id             : 00:00:00:00:00:00:00:01
16      GMC Id                : 00:00:00:00:00:00:00:01   GMC Class        : 6 (Tx: 6)
17      GMC Accuracy          : 33                        GMC Variance     : 20061
18      GMC Priority1         : 128                       GMC Priority2    : 1
19      Global Data:
20      UTC Offset            : 37                        Leap-59          : FALSE
21      Leap-61               : FALSE                     Time traceable   : TRUE
22      Freq Traceable        : TRUE                      Time Scale       : TRUE
23      Time source           : 32                        Path Trace count : 0
```

Example 3.9 Output of clock detail on R1

```
24      user@R1# run show ptp clock detail
25      Clock Details:

26      Slot Number           : 0
27      Default Data:
28      Two-step Clock        : FALSE                      Clock Identity :
e8:b6:c2:ff:fe:b7:42:f0
29      Total Ports on Device : 0                          Clock Class    : 248
30      Clock Accuracy        : 254                        Log Variance   : 15353
31      Clock Priority1       : 128                        Clock Priority2: 128
32      UTC Offset            : 37                         Leap59         : FALSE
33      Leap61                : FALSE                      Time Traceable : FALSE
34      Frequency Traceable   : FALSE                      Time Source    : 160
35      Delay Req Sending Time: 0                          Steps Removed  : 2
36      Slave-only            : FALSE
37      Parent Data:
```

```
38        Parent Id             : 08:b2:58:ff:fe:e2:d7:d0
39        GMC Id                : 00:00:00:00:00:00:00:01   GMC Class        : 6 (Tx: 6)
40        GMC Accuracy          : 33                        GMC Variance     : 20061
41        GMC Priority1         : 128                       GMC Priority2    : 1
42        Global Data:
43        UTC Offset            : 37                        Leap-59          : FALSE
44        Leap-61               : FALSE                     Time traceable   : TRUE
45        Freq Traceable        : TRUE                      Time Scale       : TRUE
46        Time source           : 32                        Path Trace count : 0
```

Example 3.10 Output of clock detail on R2

```
47        user@R2# run show ptp clock detail
48        Clock Details:

49        Slot Number           : 0
50        Default Data:
51        Two-step Clock        : FALSE                      Clock Identity :
dc:38:e1:ff:fe:12:af:d0
52        Total Ports on Device : 0                          Clock Class    : 248
53        Clock Accuracy        : 254                        Log Variance   : 15353
54        Clock Priority1       : 128                        Clock Priority2: 128
55        UTC Offset            : 37                         Leap59         : FALSE
56        Leap61                : FALSE                      Time Traceable : FALSE
57        Frequency Traceable   : FALSE                      Time Source    : 160
58        Delay Req Sending Time: 0                          Steps Removed  : 3
59        Slave-only            : FALSE
60        Parent Data:
61        Parent Id             : e8:b6:c2:ff:fe:b7:42:f0
62        GMC Id                : 00:00:00:00:00:00:00:01   GMC Class        : 6 (Tx: 6)
63        GMC Accuracy          : 33                        GMC Variance     : 20061
64        GMC Priority1         : 128                       GMC Priority2    : 128
65        Global Data:
66        UTC Offset            : 37                        Leap-59          : FALSE
67        Leap-61               : FALSE                     Time traceable   : TRUE
68        Freq Traceable        : TRUE                      Time Scale       : TRUE
69        Time source           : 32                        Path Trace count : 0
```

Example 3.11 Output of clock detail on R3

```
70        user@R3# run show ptp clock detail
71        Clock Details:

72        Slot Number           : 0
73        Default Data:
74        Two-step Clock        : FALSE                 Clock Identity : dc:38:e1:ff:fe:12:87:d0
75        Total Ports on Device : 0                          Clock Class    : 248
76        Clock Accuracy        : 254                        Log Variance   : 15353
77        Clock Priority1       : 128                        Clock Priority2: 128
78        UTC Offset            : 37                         Leap59         : FALSE
79        Leap61                : FALSE                      Time Traceable : FALSE
80        Frequency Traceable   : FALSE                      Time Source    : 160
81        Delay Req Sending Time: 0                          Steps Removed  : 4
82        Slave-only            : FALSE
83        Parent Data:
84        Parent Id             : dc:38:e1:ff:fe:12:af:d0
85        GMC Id                : 00:00:00:00:00:00:00:01   GMC Class        : 6 (Tx: 6)
86        GMC Accuracy          : 33                        GMC Variance     : 20061
87        GMC Priority1         : 128                       GMC Priority2    : 1
88        Global Data:
89        UTC Offset            : 37                        Leap-59          : FALSE
90        Leap-61               : FALSE                     Time traceable   : TRUE
91        Freq Traceable        : TRUE                      Time Scale       : TRUE
92        Time source           : 32                        Path Trace count : 0
```

In the output of Example 3.8-3.11, you can obtain information on the clock parameters advertised by each T-BC when the local clock is in the phase-aligned state:

- Lines16, 39, 62, and 85 display the `GMC Id (00:00:00:00:00:00:00:01)` and the Rx/Tx `GMC Class (6/6)` on R0/R1/R2/R3 from their upstream. It is clear that all the T-BCs are tracking the grandmaster clock.
- The `Steps Removed` (lines 12, 35, 58, and 81) are shown as 1, 2, 3, and 4, respectively, indicating that it is increased by 1 on each hop.
- The `Parent Id` (line numbers 15, 38, 61, and 84) of each T-BC is the `Clock Identity` of its immediate upstream master.

Now let's see what happens if T-BC loses packets from its upstream master. This can be simulated by stopping the PTP packets on port P1 of the tester or by various other means. When R0 stops receiving the PTP packet from its upstream, it moves to `holdover` mode as shown in Example 3.12. It is important to note that the physical layer frequency remains undisturbed.

Example 3.12 Output of lock-status during holdover on R0

```
1        user@R0# run show ptp lock-status detail
2        Lock Status:

3        Lock State    : 2 (HOLDOVER)
4        Phase offset  : 0.000000011 sec
5        State since   : 2020-07-10 23:43:28 PDT (00:00:29 ago)

6        Selected Master Details:
7        Upstream Master address    : 08:b2:58:ff:fe:e2:d7:d0
8        Slave interface            : xe-0/0/1.0
9        Clock reference state      : Clock locked
10       1pps reference state       : Clock qualified
```

The output phase from the device in this state is purely a function of the accuracy of the physical layer frequency that aids the local clock to maintain the output phase for a sufficiently longer period of time. This is called *Assisted Holdover*. Let's look at the clock parameters of the clock in this state in Example 3.13.

Example 3.13 Output of clock detail during holdover on R0

```
1        user@R0# run show ptp clock detail
2        Clock Details:

3        Slot Number           : 0
4        Default Data:
5        Two-step Clock        : FALSE                    Clock Identity :
08:b2:58:ff:fe:e2:d7:d0
6        Total Ports on Device : 0                        Clock Class    : 248
7        Clock Accuracy        : 254                      Log Variance   : 15353
8        Clock Priority1       : 128                      Clock Priority2: 128
9        UTC Offset            : 37                       Leap59         : FALSE
10       Leap61                : FALSE                    Time Traceable : FALSE
11       Frequency Traceable   : FALSE                    Time Source    : 160
12       Delay Req Sending Time: 0                        Steps Removed  : 0
```

```
13        Slave-only            : FALSE
14        Parent Data:
15        Parent Id             : 08:b2:58:ff:fe:e2:d7:d0
16        GMC Id                : 08:b2:58:ff:fe:e2:d7:d0   GMC Class        : 248 (Tx: 248)
17        GMC Accuracy          : 254                       GMC Variance     : 15353
18        GMC Priority1         : 128                       GMC Priority2    : 128
19        Global Data:
20        UTC Offset            : 37                        Leap-59          : FALSE
21        Leap-61               : FALSE                     Time traceable   : FALSE
22        Freq Traceable        : TRUE                      Time Scale       : FALSE
23        Time source           : 160                       Path Trace count : 0
```

And a few observations while the device R0 is in holdover state:

- The local clock class attribute has changed from 6 to 248 and the same is advertised through the announce message by the PTP master port.
- The `Freq Traceable` Flag is set to `TRUE`. This is an indication of the existence of a valid physical layer frequency source.
- The value of `Steps Removed` is changed to 0.
- The `GMC Id` is same as the local `Clock Identity`.
- The `GMC Priority2` has changed to the locally configured Priority2.
- Time traceable flag is reset to `FALSE`.

The output in Example 3.14 indicates that the phase plane is in holdover state and the frequency plane is in locked state.

Example 3.14 Output of PTP hybrid status on R0

```
1         user@R0# run show ptp hybrid status
2         Hybrid Mode Status:
3         Configured Mode                : Hybrid
4         Operating  Mode                : Hybrid
5         PTP Reference                  : 00:00:00:00:00:00:00:01, xe-0/0/1.0
6         Synchronous Ethernet Reference : xe-0/0/1
7         Lock state                     : Holdover
8         Lock state description         : Frequency Locked Phase Holdover
```

Let's resume the PTP transmission from the upstream master. Now the local clock should move to the acquiring state and re-establish the time with that of the master clock. During this state, the port in master state on R0 advertises the announce message based on the local clock quality until it is phase-aligned. Let's observe the output by running the commands on R0 as in Examples 3.15-3.18.

Example 3.15 Output of lock-status during Acquiring mode on R0

```
1         user@R0# run show ptp lock-status detail
2         Lock Status:

3         Lock State    : 3 (ACQUIRING)
4         Phase offset  : 0.000000011 sec
5         State since   : 2020-07-10 23:47:48 PDT (00:00:08 ago)

6         Selected Master Details:
7         Upstream Master address    : 00:00:00:00:00:00:00:01
8         Slave interface            : xe-0/0/1.0
9         Clock reference state      : Clock locked
10        1pps reference state       : Clock qualified
```

Example 3.16 Output of clock detail during Acquiring mode on R0

```
11      user@R0# run show ptp clock detail
12      Clock Details:

13      Slot Number           : 0
14      Default Data:
15      Two-step Clock        : FALSE                      Clock Identity :
08:b2:58:ff:fe:e2:d7:d0
16      Total Ports on Device : 0                          Clock Class    : 248
17      Clock Accuracy        : 254                        Log Variance   : 15353
18      Clock Priority1       : 128                        Clock Priority2: 1
19      UTC Offset            : 37                         Leap59         : FALSE
20      Leap61                : FALSE                      Time Traceable : FALSE
21      Frequency Traceable   : FALSE                      Time Source    : 160
22      Delay Req Sending Time: 0                          Steps Removed  : 1
23      Slave-only            : FALSE
24      Parent Data:
25      Parent Id             : 00:00:00:00:00:00:00:01
26      GMC Id                : 00:00:00:00:00:00:00:01   GMC Class        : 248 (Tx: 248)
27      GMC Accuracy          : 33                         GMC Variance     : 15353
28      GMC Priority1         : 128                        GMC Priority2    : 1
29      Global Data:
30      UTC Offset            : 37                         Leap-59          : FALSE
31      Leap-61               : FALSE                      Time traceable   : TRUE
32      Freq Traceable        : TRUE                       Time Scale       : TRUE
33      Time source           : 32                         Path Trace count : 0
```

Example 3.17 Output of ptp-port on R0

```
34      user@R0# run show ptp port
35      PTP port-data:
36      Local Interface   : xe-0/0/1.0
37      Local Address     : 08:b2:58:e2:d0:32
38      Remote Address    : 01:1b:19:00:00:00
39      Clock Stream      : 0              Clock Identity    : 08:b2:58:ff:fe:e2:d7:d0
40      Port State        : Slave          Delay Req Interval: -4
41      Announce Interval : 1              Announce Timeout  : 3
42      Sync Interval     : -6             Delay Mechanism   : End-to-end
43      Port Number       : 1              Operating Mode    : BMC Mode
44      Local Priority    : <not applicable>

45      Local Interface   : xe-0/0/2.0
46      Local Address     : 08:b2:58:e2:d0:31
47      Remote Address    : 01:80:c2:00:00:0e
48      Clock Stream      : 5              Clock Identity    : 08:b2:58:ff:fe:e2:d7:d0
49      Port State        : Master         Delay Req Interval: -4
50      Announce Interval : 1              Announce Timeout  : 3
51      Sync Interval     : -6             Delay Mechanism   : End-to-end
52      Port Number       : 3              Operating Mode    : Master Only
53      Local Priority    : <not applicable>
```

Example 3.18 Output of lock-status during Phase-aligned state on R0

```
54      user@R0# run show ptp lock-status detail
55      Lock Status:

56      Lock State    : 5 (PHASE ALIGNED)
57      Phase offset  : 0.000000011 sec
58      State since   : 2020-07-10 23:49:08 PDT (00:01:46 ago)

59      Selected Master Details:
60      Upstream Master address    : 00:00:00:00:00:00:00:01
61      Slave interface            : xe-0/0/1.0
62      Clock reference state      : Clock locked
63      1pps reference state       : Clock qualified
```

NOTE The MX Series platform expects `synchronous-ethernet-mapping` configuration while enabling hybrid mode with the default profile, IEEE-2008. However, for other profiles, such as G.8275.1 and G.8275.1.enh, this specific configuration is not allowed, and you should enable the hybrid mode using the `slave hybrid` knob.

NOTE With the default profile, the stateful port configuration is not supported on the MX Series platform for PTP over Ethernet and PTP over IPv4 transport. However, ACX devices ACX2100, ACX2200, ACX1100, ACX1000, ACX500, and ACX4000 support stateful port configuration with the default profile and PTP over Ethernet transport.

Let's now look at the various state of the local clock based on the values of the announce message with a default profile.

Table 3.9 Tx Announce Message Content-default Profile

Announce Message Field	Local Clock State			
	Freerun	**Acquiring**	**Locked**	**Holdover**
sourcePortIdentity	**Local clockId of the T-BC + Port Number**	**Local clockId of the T-BC + Port Number**	**Local clockId of the T-BC + Port Number**	**Local clockId of the T-BC + Port Number**
Leap61/leap59	**FALSE**	**(Note 1)**	**(Note 1)**	**TRUE/FALSE (Note 2)**
currentUtcOffsetValid	**FALSE**	**(Note 1)**	**(Note 1)**	**TRUE/FALSE (Note 2)**
ptpTimescale	**TRUE**	**TRUE**	**(Note 1)**	**TRUE**
timeTraceable	**FALSE**	**Previous State**	**(Note 1)**	**FALSE**
frequencyTraceable	**Based on Frequency Source Lock**	**Based on Frequency Source Lock**	**(Note 1)**	**Based on Frequency Source Lock**
currentUtcOffset	**Last UTC offset**	**Last UTC offset**	**(Note 1)**	**Last UTC offset**
grandmasterPriority1	**128 (default)**	**128 (default)**	**(Note 1)**	**128 (default)**
grandmasterClockQuality. clockClass	**248**	**248**	**(Note 1)**	**248**
grandmasterClockQuality. clockAccuracy	**0xFE**	**0xFE**	**(Note 1)**	**0xFE**
grandmasterClockQuality. offsetScaledLogVariance	**0xFFFF**	**0xFFFF**	**(Note 1)**	**0xFFFF**
grandmasterPriority2	**Configured Priority2 of T-BC**	**Configured Priority2 of T-BC**	**(Note 1)**	**Configured Priority2 of T-BC**
grandmasterIdentity	**Local clockId of the T-BC**	**Local clockId of the T-BC**	**(Note 1)**	**Local clockId of the T-BC**
stepsRemoved	**0**	**0**	**Received stepsRemoved +1**	**0**
timeSource	**0xA0**	**0xA0**	**(Note 1)**	**0xA0**

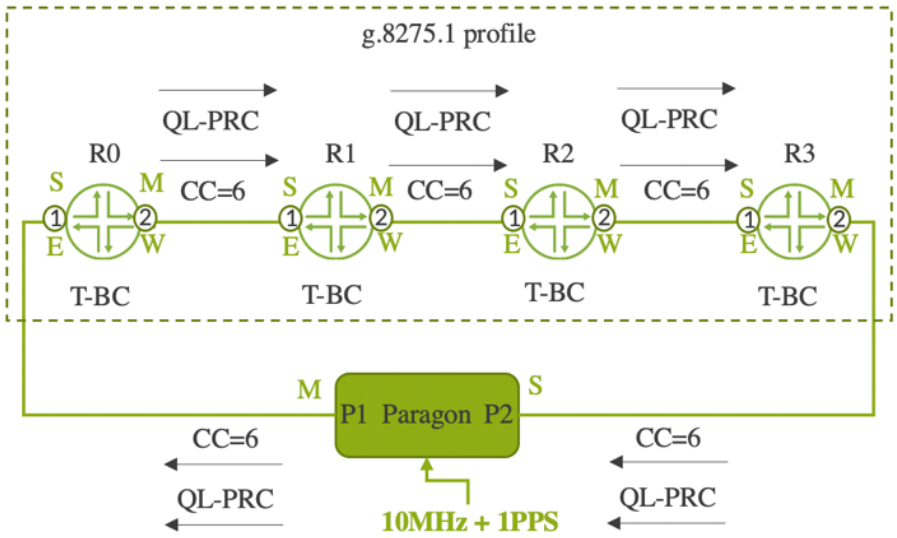
Note 1 – The value sent in the announce message corresponds to the value of the current grandmaster.

Note 2 – As per PTP. Usually that of previously locked grandmaster.

Chain of T-BCs with g.8275.1-profile for Phase/Time

Figure 3.6 shows the configuration of the g.8275.1 profile and clock advertisement along the chain of T-BCs.

Figure 3.6 T-BCs with g.8275.1 Profile



Referring to the configuration of PTP over IEEE802.3 Ethernet transport with default profile (as mentioned in *Example 3.1)*, the G.8275.1 profile configuration on the MX Series platform requires two changes as shown in *Example 3.19*: the profile name (line 3) and the hybrid configuration (lines 6 and 21).

Example 3.19 Configuration of g.8275.1 profile on R0

```
1         user@R0# show protocols ptp
2         clock-mode boundary;
3         profile-type g.8275.1;
4         priority2 1;
5         phy-timestamping;
6         slave {
7             interface xe-0/0/1.0 {
8                 multicast-mode {
9                     transport {
10                        ieee-802.3;
11                    }
12                }
13            }
21            hybrid;
22        }
23        master {
18            interface xe-0/0/2.0 {
19                multicast-mode {
20                    transport {
21                        ieee-802.3 link-local;
22                    }
23                }
24            }
32        }
```

In Example 3.19's configuration, the PTP port state is explicitly configured as client and master. ITU-T standard doesn't specify the client-only PTP port. It specifies either stateful or master only on PTP ports. However, the MX Series platform currently supports client only, master only, and stateful PTP port configurations with the g.8275.1 profile.

NOTE The MX Series platform doesn't support coexisting client and stateful PTP port configurations with g.8275.1 profile. The supported configuration options for the PTP port are:

- Client and master configurations,
- Stateful configurations, and
- Stateful and master configurations

Now let's look at the g.8275.1 profile configuration using the `stateful` knob as shown in Example 3.20. Here, both xe-0/0/1 and xe-0/0/2 ports are configured as stateful ports. Based on the state decision and data set comparison algorithms, the port states are determined as client, master, and passive.

Example 3.20 Configuration of g.8275.1 profile on R0

```
user@R0# show protocols ptp
clock-mode boundary;
profile-type g.8275.1;
priority2 1;
phy-timestamping;
slave {
    hybrid;
}
stateful {
    interface xe-0/0/1.0 {
        multicast-mode {
            transport {
                ieee-802.3 link-local;
            }
        }
    }
    interface xe-0/0/2.0 {
        multicast-mode {
            transport {
                ieee-802.3 link-local;
            }
        }
    }
}
```

NOTE ACX710 platform doesn't support T-TSC clock mode with g.8275.1 profile.

NOTE ACX710 platform support the following configuration options with g.8275.1 profile in T-BC clock mode.

- Stateful configuration
- Stateful and Master configurations

NOTE Configuration CLI for g.8275.1 profile on ACX710 platform is slightly different as compared to MX platform. Here, both stateful and Master configurations are configured using stateful knob. When specified explicitly the knob `slave-candidate` under stateful configurations, it function as stateful BMCA port, similar to that in MX. If you don't specify the `slave-candidate` knob under stateful configuration, then the corresponding port behave as Master port.

Let's look at the g.8275.1 profile configuration on ACX710 platform as shown in *Example 3.21*.

Example 3.21 Configuration of g.8275.1 profile on ACX710

```
user@R0# show protocols ptp
clock-mode boundary;
profile-type g.8275.1;
priority2 1;
stateful {
    interface xe-0/0/1.0 {
        multicast-mode {
            slave-candidate;
            transport {
                ieee-802.3 link-local;
            }
        }
    }
    interface xe-0/0/2.0 {
        multicast-mode {
            slave-candidate;
            transport {
                ieee-802.3 link-local;
            }
        }
    }
}
```

You can see the following differences on ACX710 configurations as compared to MX:

- No configuration needed for phy-timestamping. It is enabled by default on the ACX710.
- No explicit configuration needed for hybrid mode. Device operate in hybrid mode, when both PTP and SyncE configurations are committed successfully.
- Additional configuration knob `slave-candidate` is mandatory to operate the port in stateful BMCA mode. Without this knob, the PTP port will act in master-only mode.
- A new CLI knob `acquiring-state-announce-grandmaster` is added under the hierarchy `set protocols ptp stateful`. This will enable the Tx announce-message content based on grandmaster data-set while the device is in Acquiring state.
- A new CLI knob for configuring VLAN and priority under PTP stanza. User should make sure that the configured IFL VLAN and PTP VLAN are same.

- A new CLI knob `holdover-time-error-budget` is added under the hierarchy `set protocols ptp`. This will help user to configure the hold-over-in-specification time error budget. The range supported is (0 to 10000).
- Another difference in ACX710 is the support for per stream configuration for packet rates.

Let's go back to Figure 3.6 and look at the PTP configurations needed on devices R1 through R3 in Examples 3.22-3.24. To avoid repetition, the SyncE configurations are not added (see configuration Example 3.2).

Example 3.22 Configuration of g.8275.1 profile on R1

```
1        user@R1# show protocols ptp
2        clock-mode boundary;
3        profile-type g.8275.1;
4        priority2 1;
5        phy-timestamping;
6        slave {
7            hybrid;
8        }
9        stateful {
10           interface xe-0/0/1.0 {
11               multicast-mode {
12                   transport {
13                       ieee-802.3 link-local;
14                   }
15               }
16           }
17           interface xe-0/0/2.0 {
18               multicast-mode {
19                   transport {
20                       ieee-802.3 link-local;
21                   }
22               }
23           }
24       }
```

Example 3.23 Configuration of g.8275.1 profile on R2

```
25       user@R2# show protocols ptp
26       clock-mode boundary;
27       profile-type g.8275.1;
28       priority2 1;
29       phy-timestamping;
30       slave {
31           hybrid;
32       }
33       stateful {
34           interface xe-0/0/1.0 {
35               multicast-mode {
36                   transport {
37                       ieee-802.3 link-local;
38                   }
39               }
40           }
41           interface xe-0/0/2.0 {
42               multicast-mode {
43                   transport {
44                       ieee-802.3 link-local;
45                   }
46               }
47           }
48       }
```

Example 3.24 Configuration of g.8275.1 profile on R3

```
49        user@R3# show protocols ptp
50        clock-mode boundary;
51        profile-type g.8275.1;
52        priority2 1;
53        phy-timestamping;
54        slave {
55            hybrid;
56        }
57        stateful {
58            interface xe-0/0/1.0 {
59                multicast-mode {
60                    transport {
61                        ieee-802.3 link-local;
62                    }
63                }
64            }
65            interface xe-0/0/2.0 {
66                multicast-mode {
67                    transport {
68                        ieee-802.3 link-local;
69                    }
70                }
71            }
72        }
```

Let's now look at the PTP port details on R0 and verify the port status by issuing the commands in Example 3.25. The output indicates many port attributes, mainly the `Operating Mode` of the ports, configured port rates, `Clock Stream`, `Port Number`, `Local Priority`, etc.

Example 3.25 PTP Port Details on R0

```
1         user@R0# run show ptp port
2         PTP port-data:
3         Local Interface   : xe-0/0/1
4         Local Address     : ea:b6:c2:b7:3b:33
5         Remote Address    : 01:80:c2:00:00:0e
6         Clock Stream      : 5              Clock Identity    : e8:b6:c2:ff:fe:b7:42:f0
7         Port State        : Slave          Delay Req Interval: -4
8         Announce Interval : -3             Announce Timeout  : 3
9         Sync Interval     : -4             Delay Mechanism   : End-to-end
10        Port Number       : 2              Operating Mode    : Stateful
11        Local Priority    : 128

12        Local Interface   : xe-0/0/2
13        Local Address     : ea:b6:c2:b7:3b:35
14        Remote Address    : 01:80:c2:00:00:0e
15        Clock Stream      : 4              Clock Identity    : e8:b6:c2:ff:fe:b7:42:f0
16        Port State        : Master         Delay Req Interval: -4
17        Announce Interval : -3             Announce Timeout  : 3
18        Sync Interval     : -4             Delay Mechanism   : End-to-end
19        Port Number       : 1              Operating Mode    : Stateful
20        Local Priority    : 128
```

The clock specification standard G.8273.2 specifies two types of holdover specifications:

- Assisted holdover, and
- Unassisted holdover.

In assisted holdover, the local clock remains in holdover with a valid physical layer frequency reference that helps maintain the correct time over a longer period.

In unassisted holdover, the local clock is in holdover without any physical layer frequency reference.

The G.8275.1 profile also specifies two types of holdover specifications:

- Holdover-in-specification, and
- Holdover-out-specification.

If the local clock is within the holdover budget, and a typical value is 400 nsec, then it remains in holdover-in-specification. If the phase error exceeds the holdover budget, then it changes its state to holdover-out-specification. Let's now look at the various states of the local clock based on the values of the announce message.

NOTE As of the writing of this book, only the ACX710 platform supports the holdover-in-specification and holdover-out-specification states under ptp lock-status. However, the Clock Class values corresponding to these states are supported on both ACX710 and MX platforms.

Table 3.10 Tx Announce Message Content-G.8275.1 Profile

Announce Message field	Local Clock State				
	Free-run	**Acquiring**	**Locked**	**Holdover-in-spec**	**Holdover-out-spec**
sourcePortIdentity	**Local clockId of the T-BC + Port Number**	**Local clockId of the T-BC + Port Number**	**Local clockId of the T-BC + Port Number**	**Local clockId of the T-BC + Port Number**	**Local clockId of the T-BC + Port Number**
Leap61/leap59	**FALSE**	**(Note 1)**	**(Note 1)**	**TRUE/FALSE (Note 2)**	**TRUE/FALSE (Note 2)**
currentUtcOffsetValid	**FALSE**	**Previous State**	**(Note 1)**	**TRUE/FALSE (Note 2)**	**TRUE/FALSE (Note 2)**
ptpTimescale	**TRUE**	**TRUE**	**(Note 1)**	**TRUE**	**TRUE**
timeTraceable	**FALSE**	**Previous State**	**(Note 1)**	**TRUE**	**FALSE**
frequencyTraceable	**Based on Frequency Source Lock**	**Based on Frequency Source Lock**	**(Note 1)**	**Based on Frequency Source Lock**	**Based on Frequency Source Lock**
currentUtcOffset	**As per PTP**	**Last known UTC offset**	**(Note 1)**	**Last known UTC offset**	**Last known UTC offset**
grandmasterPriority1	**128 (default)**	**128 (default)**	**(Note 1)**	**128 (default)**	**128 (default)**
grandmasterClockQuality.clockClass	**248**	**Previous state 135/165/248**	**(Note 1)**	**135**	**165**
grandmasterClockQuality.clockAccuracy	**0xFE**	**0xFE**	**(Note 1)**	**0xFE**	**0xFE**
grandmasterClockQuality.offsetScaledLogVariance	**0xFFFF**	**0xFFFF**	**(Note 1)**	**0xFFFF**	**0xFFFF**

grandmasterPriority2	**Configured Priority2 of T-BC**	**Configured Priority2 of T-BC**	**(Note 1)**	**Configured Priority2 of T-BC**	**Configured Priority2 of T-BC**
grandmasterIdentity	**Local clockId of the T-BC**	**Local clockId of the T-BC**	**(Note 1)**	**Local clockId of the T-BC**	**Local clockId of the T-BC**
stepsRemoved	**0**	**0**	**Received stepsRemoved +1**	**0**	**0**
timeSource	**0xA0**	**0xA0**	**(Note 1)**	**0xA0**	**0xA0**
synchronizationUncertain	**TRUE**	**TRUE**	**(Note 3)**	**(Note 3)**	**(Note 3)**

Note 1 – The value sent in the announce message corresponds to the value of the current grandmaster or Time interface in case T-BC has selected a virtual port as best master.

Note 2 – Refer to Table A.8 of g.8275.1 standard.

Note 3 – The value sent in the Announce message corresponds to the value received from the current parent clock.

Virtual Port Configuration with G.8275.1 Profile

NOTE At the time of the writing of this book, the ACX710 doesn't claim support of virtual-port. This feature will be available in upcoming releases. However, for completeness, we are covering the feature in this section.

When the T-BC acts as a Telecom-Grand Master (T-GM) with an external phase/time input coming from a PRTC, it is handled by means of a virtual port. The Juniper ACX710 platform supports the virtual port with G.8275.1 profile using an external GNSS receiver as PRTC. The GNSS receiver is connected to the GPS antenna at its input and provides TOD and 1PPS signal output to the ACX710 via a RJ45 TOD port in the front-panel. In normal scenarios, the ABMCA on R3 selects the virtual port for clock recovery and transmits the recovered clock to BS1 or any downstream T-BCs. In the event of a GNSS failover, R3 recovers the clock from the backup PTP path and delivers phase and frequency to downstream devices.

NOTE At the time of the writing of this book, the ACX710 doesn't support the APTS model with external GNSS receiver. This means the local clock doesn't go to assisted holdover with the support of the available physical layer frequency from the backup path. Look for this to be supported in future releases.

Figure 3.7 T-BCs with g.8275.1 Profile and Virtual Port

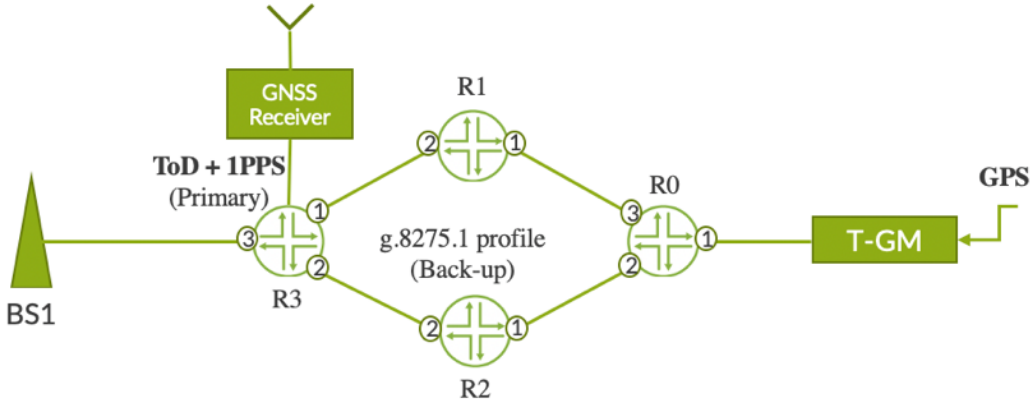


Figure 3.7 illustrates the virtual port functionality. The minimum configuration required to enable virtual port functionality on R3 is mentioned below. When compared to the standard g.8275.1 profile configurations, line 5 and lines 27-40 are the additional configuration required for enabling virtual port functionality. Configuration on R0 through R2 remains same as that of g.8275.1 profile.

Example 3.26 Configuration of virtual port in g.8275.1 profile on R3

```
1         user@R3# show protocols ptp
2         clock-mode boundary;
3         profile-type g.8275.1;
4         priority2 10;
5         virtual-port;
6         stateful {
7             interface xe-0/0/1.0 {
8                 multicast-mode {
9                     slave-candidate;
10                    transport {
11                        ieee-802.3;
12                    }
13                }
14            }
15            interface xe-0/0/2.0 {
16                multicast-mode {
17                    slave-candidate;
18                    transport {
19                        ieee-802.3;
20                    }
21                }
22            }
23        }
```

Example 3-27 Configuration of chassis synchronization on R3

```
24        user@R3# show chassis synchronization
25        network-option option-1;
26        selection-mode received-quality;
27        clock-mode auto-select;
28        port auxiliary {
29            client {
30                time-of-day-format {
31                    nmea-custom-format;
32                }
33                constellation gps-beidou;
34                dump-gpsstats;
```

```
35          }
36      }
37      source {
38          virtual-port {
39              wait-to-restore 0;
40              quality-level prc;
41          }
42      }
43          interfaces xe-0/0/1 {
44              wait-to-restore 0;
45              quality-level prc;
46          }
47      }
48          interfaces xe-0/0/2 {
49              wait-to-restore 0;
50              quality-level prc;
51          }
52      }
53      esmc-transmit {
54          interfaces all;
55      }
```

Let's verify the clock status by issuing the following commands and confirm that the local clock is indeed aligned in phase/frequency with respect to the local time reference, 1PPS + TOD in this case. Line 5 clearly indicates that the selected `Source is Virtual Port`. Lines 11 through 13 indicate the `Configured ports` and `Rx status`.

Example 3.28 Output of PTP lock status with virtual port on R3

```
1       user@R3# run show ptp lock-status detail
2       Lock Status:

3       Lock State    : 5 (PHASE ALIGNED)
4       State since   : 2020-07-24 04:31:14 PDT (00:05:02 ago)
5       Source        : Virtual Port
```

Example 3.29 Output of chassis synchronization on R3

```
6       user@R3# run show chassis synchronization extensive
7       Current clock status  : Locked
8       Clock locked to       : Primary
9       SNMP trap status      : Disabled

10      Configured ports:

11      Name                : auxiliary
12      Rx status           : active
13      UTC Offset          : 37

14      Configured sources:

15      Interface           : virtual-port
16      Status              : Primary       Index       : 1
17      Clock source state  : Clk qualified Priority    : Default(6)
18      Configured QL       : prc         ESMC QL     : PRC
19      Clock source type   : GNSS          Clock Event : Clock locked
20      Wait-to-restore     : 0  min        Hold-off    : 1000 ms
21      Interface State     : Up,pri,ESMC Rx(SSM 0x2),

22      Interface           : xe-0/0/1
23      Status              : Secondary     Index       : 153
24      Clock source state  : Clk qualified Priority    : Default(8)
25      Configured QL       : prc           ESMC QL     : n/a
26      Clock source type   : ifd           Clock Event : Clock qualified
```

```
27        Wait-to-restore     : 0  min        Hold-off    : 1000 ms
28        Interface State     : Up,sec,ESMC Rx(SSM 0xb),ESMC TX(QL PRC/SSM 0x2),

29        Interface           : xe-0/0/2
30        Status              : n/a           Index       : 154
31        Clock source state  : n/a           Priority    : Default(8)
32        Configured QL       : prc           ESMC QL     : n/a
33        Clock source type   : ifd           Clock Event : n/a
34        Wait-to-restore     : 0  min        Hold-off    : 1000 ms
35        Interface State     : Up,ESMC Rx(SSM 0xb),ESMC TX(QL PRC/SSM 0x2),
```

Example 3.30 Output of GRU status with virtual port on R3

```
36        user@R3# run show chassis synchronization gru extensive
37        Current ToD              : 06:06:39 25/07/2020
38        Current TAI              : 06:06:58 25/07/2020
39        Current UTC              : 06:06:21 25/07/2020
40        TOD Protocol             : nmea-custom-format
41        Port Status              : ON
42        Port Details             : RS422 9600 bps
43        Alarms                   : NONE
44        Antenna DC Status        : 2 (Nominal current detected)
45        Constellation-Wanted     : gps-beidou
46        Constellation-Actual     : gps-beidou
47        GPSS Status              : 0 (Locked)
48        GPSS Faulty              : 0 (GPS Receiver up and running)
49        PPS SM Mode              : 2 (Position_hold-Mode)
50        GPS Quality              : 1 (Standalone GPS positioning)
51        1PPS Loopback            : Not Enabled
52        1PPS Counts              : 318168
53        Cable Delay Compensation : 0
54        Antenna Cable Delay      : 0
55        Self Survey Length       : 2000
56        Reset Last Received      : 00:00:00 00/00/0000
57        Reason For Last Reset    : 8
58        Product Designation      : GRU 04 01
59        Product No.              : NCD 901 65/1
60        Product Rev              : R1E
61        Additional Information   : E640000586.1927
62        GRM Hardware ID          : NA
63        GRM Serial Number        : NA
64        GRM Manf Date            : NA
65        GRM Firmware Version     : NA
66        Client                   : 98:a4:04:7d:d2:ff
67        Client In Control        : 98:a4:04:7d:d2:ff

68        Received Sentences:
69        PREC, GPppr              : 317509
70        PERC, GPsts              : 317509
71        PERC, GPver              : 5291
72        PERC, GPrst              : 0
73        PERC, GPssl              : 10574
74        PERC, GPdly              : 10583
75        PERC, GPavp              : 5291
76        PERC, GPtsp              : 0
77        GPGSV                    : 14078
78        GPGSA                    : 5290
79        BDGSV                    : 19643
80        BDGSA                    : 0
81        GLGSV                    : 0
82        GLGSA                    : 7690
83        GAGSV                    : 0
84        GAGSA                    : 0
85        QZGSV                    : 0
86        QZGSA                    : 0
87        GPGGA                    : 5290
```

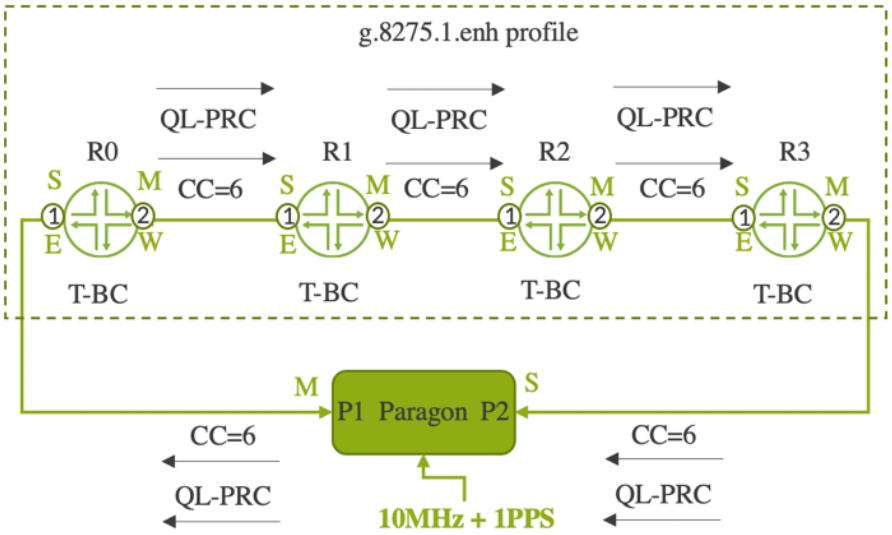
```
88      GPCTR                   : 10581
89      Other                   : 0
90      Protocol Errors:
91      Unexpected Characters   : 0
92      Checksum Error          : 4
93      Format Error            : 0
94      Other Error             : 0

95      No. of Satellites Used  : 19

96      Visible Satellite List:

97      Sat No    Signal Level     Status        Type
98      5         43    dBHZ       Acquired      GPS
99      2         43    dBHZ       Acquired      GPS
100     13        42    dBHZ       Acquired      GPS
101     17        40    dBHZ       Acquired      GPS
102     19        39    dBHZ       Acquired      GPS
103     25        38    dBHZ       Acquired      GPS
104     6         38    dBHZ       Acquired      GPS
105     223       41    dBHZ       Acquired      BEIDOU
106     202       39    dBHZ       Acquired      BEIDOU
107     228       39    dBHZ       Acquired      BEIDOU
108     213       38    dBHZ       Acquired      BEIDOU
109     205       38    dBHZ       Acquired      BEIDOU
110     210       38    dBHZ       Acquired      BEIDOU
111     201       37    dBHZ       Acquired      BEIDOU
112     203       37    dBHZ       Acquired      BEIDOU
113     208       36    dBHZ       Acquired      BEIDOU
114     225       35    dBHZ       Acquired      BEIDOU
115     209       35    dBHZ       Acquired      BEIDOU
116     227       34    dBHZ       Acquired      BEIDOU
117     216       34    dBHZ       Acquired      BEIDOU
118     207       33    dBHZ       Acquired      BEIDOU
119     206       31    dBHZ       Acquired      BEIDOU
```

Chain of T-BCs with g.8275.1.enh profile

As mentioned earlier in this chapter, the g.8275.1.enh profiles support both PTP over IPv4 and PTP over Ethernet transport (see Figure 3.8). The configuration of the g.8275.1.enh profile for Ethernet is similar to that of g.8275.1, except the `profile-type` should be configured as `g.8275.1.enh`. Therefore, in this section, you will see the configuration of g.8275.1.enh profile for PTP over IPv4 transport only. Again, to avoid repetition, the SyncE configurations are not shown but they can be reused from the default profile.

The configuration in Examples 3.31-3.34 is similar to that of the default profile except that you don't need to specify the `synchronous-ethernet-mapping configuration`. Just enable the `hybrid` knob under the `slave` stanza.

Figure 3.8 T-BCs with g.8275.1.enh Profile



Example 3.31 Configuration of g.8275.1.enh profile on R0

```
1         user@R0# show protocols ptp
2         clock-mode boundary;
3         profile-type g.8275.1.enh;
4         priority2 2;
5         phy-timestamping;
6         slave {
7             interface xe-0/0/1.0 {
8                 unicast-mode {
9                     transport ipv4;
10                    clock-source 10.0.0.1 local-ip-address 10.0.0.2;
11                }
12            }
13            hybrid;
14        }
15        master {
16            interface xe-0/0/2.0 {
17                unicast-mode {
18                    transport ipv4;
19                    clock-client 12.0.0.2/32 local-ip-address 12.0.0.1;
20                }
21            }
22        }
```

Example 3.32 Configuration of g.8275.1.enh profile on R1

```
23        user@R1# show protocols ptp
24        clock-mode boundary;
25        profile-type g.8275.1.enh;
26        priority2 2;
27        phy-timestamping;
28        slave {
29            interface xe-0/0/1.0 {
30                unicast-mode {
31                    transport ipv4;
32                    clock-source 12.0.0.1 local-ip-address 12.0.0.2;
33                }
34            }
35            hybrid;
36        }
37        master {
38            interface xe-0/0/2.0 {
39                unicast-mode {
40                    transport ipv4;
```

```
41                  clock-client 14.0.0.2/32 local-ip-address 14.0.0.1;
42              }
43          }
44      }
```

Example 3.33 Configuration of g.8275.1.enh profile on R2

```
45      user@R2# show protocols ptp
46      clock-mode boundary;
47      profile-type g.8275.1.enh;
48      priority2 2;
49      phy-timestamping;
50      slave {
51          interface xe-0/0/1.0 {
52              unicast-mode {
53                  transport ipv4;
54                  clock-source 14.0.0.1 local-ip-address 14.0.0.2;
55              }
56          }
57          hybrid;
58      }
59      master {
60          interface xe-0/0/2.0 {
61              unicast-mode {
62                  transport ipv4;
63                  clock-client 16.0.0.2/32 local-ip-address 16.0.0.1;
64              }
65          }
66      }
```

Example 3.34 Configuration of g.8275.1.enh profile on R3

```
67      user@R3# show protocols ptp
68      clock-mode boundary;
69      profile-type g.8275.1.enh;
70      priority2 2;
71      phy-timestamping;
72      slave {
73          interface xe-0/0/1.0 {
74        unicast-mode {
75                  transport ipv4;
76                  clock-source 16.0.0.1 local-ip-address 16.0.0.2;
77              }
78          }
79          hybrid;
80      }
81      master {
82          interface xe-0/0/2.0 {
83              unicast-mode {
84                  transport ipv4;
85                  clock-client 18.0.0.2/32 local-ip-address 18.0.0.1;
86              }
87          }
88      }
```

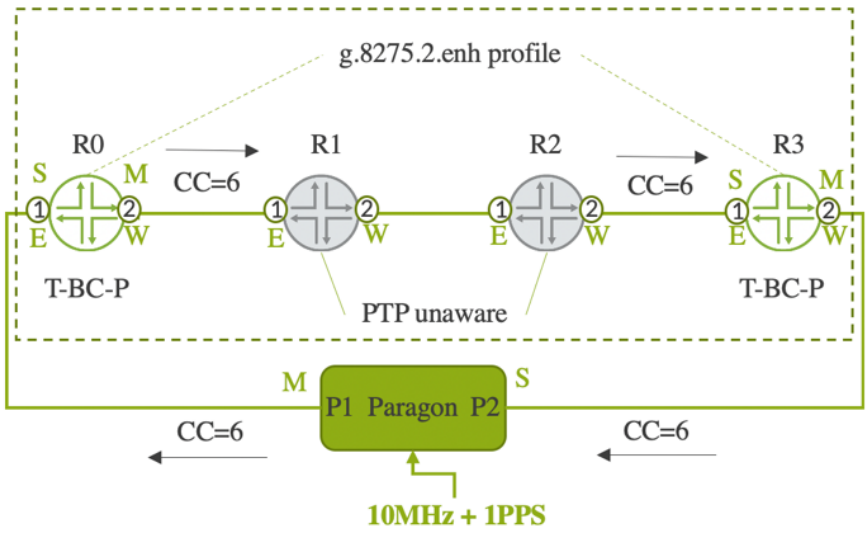
Chain of T-BCs in Partial Timing Network with g.8275.2.enh-profile

The ITU-T G.8275.2 profile is used in a network with partial timing support. In Figure 3.9, R0 and R3 are timing-aware devices that are configured with the G.8275.2.enh profile. R1 and R2 are PTP-unaware devices. The g.8275.2 profile uses unicast IPv4 and IPv6 for PTP transport. Let's now look at the g.8275.2 configurations.

First there are some noteworthy comments:

- The g.8275.2.enh profile is currently supported on ACX1100, ACX5448, ACX710, QFX5110-48s, and QFX5200-32c.
- The ACX710 uses the profile name *g.8275.2*. However, other Juniper platforms, such as the ACX5448, and the QFX Series use the profile name *g.8275.2.enh*.
- The configuration of AE interfaces is currently supported by the QFX platform, QFX5110-48s/QFX5200-32c. Forwarding of PTP packets using AE will work as with any other traffic types, unlike other profiles. Here, there is no requirement to pin the traffic over one of the physical links of AE. The default or user defined IP hashing function selects the link based on per flow parameters such as source and destination IP address, protocol type or next header, source and destination UDP port, etc. Because both transmit and receive directions will select the AE link independently, the PTP transmit and receive paths for a single PTP stream may take different physical links and thus there is a possible asymmetry in the PTP stream, causing performance degradation.
- The use of loopback for PTP will work by allowing the lo0 interface to be configured as a master or client port. An IP address configured on lo0 will be used as the local IP address in the PTP configuration statements, and the remote master or client IP will be used to identify the destination forwarding direction. Multiple IP addresses can be configured on lo0, allowing different unique PTP streams to co-exist on lo0.
- In timing-unaware devices, there is no PTP specific configuration. However, you should apply proper CoS configuration to ensure the right priority treatment for PTP packets as compared to the competing data packets.

Figure 3.9 T-BCs with g.8275.2.enh Profile



Example 3.35 Configuration of g.8275.2.enh profile on R0- IPv4 unicast

```
user@R0# show protocols ptp
clock-mode boundary;
profile-type g.8275.2.enh;
priority2 1;
domain 44;
unicast-negotiation;
slave {
    interface xe-0/0/1.0 {
        unicast-mode {
            transport ipv4;
            clock-source 10.0.0.2 local-ip-address 10.0.0.1;
        }
    }
}
master {
    interface xe-0/0/2.0 {
        unicast-mode {
            transport ipv4;
            clock-client 13.0.0.2/32 local-ip-address 11.0.0.1;
        }
    }
}
```

Example 3.36 Configuration of g.8275.2.enh profile on R3- IPv4 unicast

```
user@R3# show protocols ptp
clock-mode boundary;
profile-type g.8275.2.enh;
priority2 2;
domain 44;
unicast-negotiation;
slave {
    interface xe-0/0/1.0 {
        unicast-mode {
            transport ipv4;
            clock-source 11.0.0.1 local-ip-address 13.0.0.2;
        }
    }
}
master {
    interface xe-0/0/2.0 {
        unicast-mode {
            transport ipv4;
            clock-client 20.0.0.2/32 local-ip-address 20.0.0.1;
        }
    }
}
```

Example 3.37 Configuration of g.8275.2.enh profile on R0- IPv6 unicast

```
user@R0# show protocols ptp
clock-mode boundary;
profile-type g.8275.2.enh;
domain 44;
unicast-negotiation;
slave {
    interface xe-0/0/1.0 {
        unicast-mode {
            transport ipv6;
            clock-source 10::1 local-ip-address 10::2;
        }
    }
}
master {
    interface xe-0/0/2.0 {
```

```
16              unicast-mode {
17                  transport ipv6;
18                  clock-client 13::2/128 local-ip-address 11::1;
19              }
20          }
21      }
```

Example 3.38 Configuration of g.8275.2.enh profile on R3- IPv6 unicast

```
22      user@R3# show protocols ptp
23      clock-mode boundary;
24      profile-type g.8275.2.enh;
25      domain 44;
26      unicast-negotiation;
27      slave {
28          interface xe-0/0/1.0 {
29              unicast-mode {
30                  transport ipv6;
31                  clock-source 11::1 local-ip-address 13::2;
32              }
33          }
34      }
35      master {
36          interface xe-0/0/2.0 {
37              unicast-mode {
38                  transport ipv6;
39                  clock-client 20::2/128 local-ip-address 20::1;
40              }
41          }
42      }
```

Table 3.4, specified at the beginning of this chapter, summarizes the various configuration options of the g.8275.2.enh profile. Let's now examine some of the verification commands.

Example 3.39 PTP lock status on R0-g.8275.2.enh profile- IPv6 unicast

```
43      user@R0# run show ptp lock-status detail
44      Lock Status:

45      Lock State    : 5 (PHASE ALIGNED)
46      Phase offset  : -0.000000072 sec
47      State since   : 2020-08-20 22:33:21 PDT (00:09:38 ago)

48      Selected Master Details:
49      Upstream Master address    : 10::1
50      Slave interface            : xe-0/0/1.0
51      Clock reference state      : Clock locked
52      1pps reference state       : Clock qualified
```

Example 3.40 PTP clock detail on R0-g.8275.2.enh profile- IPv6 unicast

```
53      user@R0# run show ptp clock detail
54      Clock Details:

55      Slot Number           : 0
56      Default Data:
57      Two-step Clock        : FALSE                     Clock Identity :
e4:5d:37:ff:fe:23:d0:40
58      Total Ports on Device : 128                       Clock Class    : 248
59      Clock Accuracy        : 254                       Log Variance   : 65535
60      Clock Priority1       : 128                       Clock Priority2: 128
61      UTC Offset            : 37                        Leap59         : FALSE
62      Leap61                : FALSE                     Time Traceable : FALSE
63      Frequency Traceable   : FALSE                     Time Source    : 160
```

```
64      Delay Req Sending Time: 0                        Steps Removed  : 1
65      Slave-only            : FALSE
66      Parent Id             : 00:00:00:00:00:00:00:01
67      GMC Id                : 00:00:00:00:00:00:00:01  GMC Class        : 6 (Tx: 6)
68      GMC Accuracy          : 33 (Tx: 33)              GMC Variance     : 20061 (Tx: 20061)
69      GMC Priority1         : 128                      GMC Priority2    : 128 (Tx: 128)
70      Global Data:
71      UTC Offset            : 37                       Leap-59          : FALSE
72      Leap-61               : FALSE                    Time traceable   : TRUE
73      Freq Traceable        : TRUE                     Time Scale       : TRUE
74      Time source           : 160                      Path Trace count : 0
```

Example 3.41 Output of PTP global information on R0

```
75      user@R0# run show ptp global-information
76      PTP Global Configuration:
77      Domain number           : 44
78      Clock mode              : Boundary
79      Profile type            : G.8275.2.ENH
80      Priority Level1         : 128
81      Priority Level2         : 20
82      Local Priority          : 128
83      Path Trace              : Disabled
84      Unicast Negotiation     : Enabled
85      ESMC QL From Clock Class: Disabled
86      Clock Class/ESMC QL     :  -
87      SNMP Trap Status        : Disabled
88      PHY Time Stamping       : Disabled
89      UTC Leap Seconds        : 37
90      Transparent-clock-config : DISABLED
91      Transparent-clock-status : N/A
92        Sync Interval         : -6 (64 packets per second - unicast request)
93        Delay Request Interval: -6 (64 packets per second - unicast request)
94        Announce Interval     : 0 (1 packet per second - unicast request)
95        Announce Timeout      : 3
96        Grant Duration        : 300
97      Master Parameters:
98        Sync Interval               : -7 (128 packets per second - unicast grant)
99        Delay Request Interval      : -7 (128 packets per second - unicast grant)
100       Announce Interval           : -3 (8 packets per second - unicast grant)
101       Delay Request Timeout       : <not applicable>
102       Clock Step                  : one-step
103       Arbitrary Mode              : FALSE

104     Number of Slaves       : 1
105     Number of Masters      : 1
106     Number of Stateful     : 0
```

Example 3.42 PTP lock status on R3-g.8275.2.enh profile- IPv6 unicast

```
107     user@R3# run show ptp lock-status detail
108     Lock Status:

109     Lock State    : 5 (PHASE ALIGNED)
110     Phase offset  : -0.000000094 sec
111     State since   : 2020-08-20 22:40:11 PDT (00:04:37 ago)

112     Selected Master Details:
113     Upstream Master address    : 11::1
114     Slave interface            : xe-0/0/1.0
115     Clock reference state      : Clock locked
116     1pps reference state       : Clock qualified
```

Example 3.43 PTP clock detail on R3-g.8275.2.enh profile- IPv6 unicast

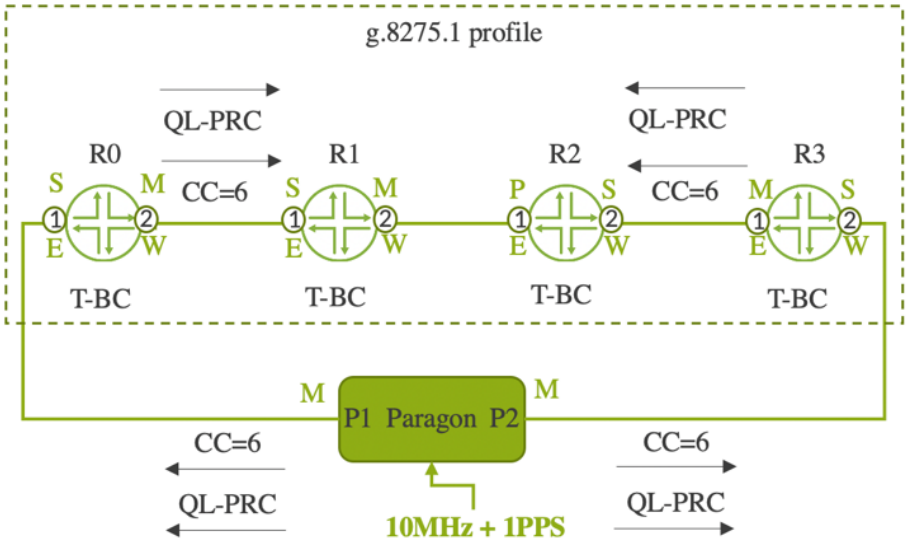
```
117     user@R3# run show ptp clock detail
118     Clock Details:
```

```
119       Slot Number           : 0
120       Default Data:
121       Two-step Clock        : FALSE                      Clock Identity :
e4:5d:37:ff:fe:23:d6:4d
122       Total Ports on Device : 128                        Clock Class    : 248
123       Clock Accuracy        : 254                        Log Variance   : 65535
124       Clock Priority1       : 128                        Clock Priority2: 128
125       UTC Offset            : 37                         Leap59         : FALSE
126       Leap61                : FALSE                      Time Traceable : FALSE
127       Frequency Traceable   : FALSE                      Time Source    : 160
128       Delay Req Sending Time: 0                          Steps Removed  : 2
129       Slave-only            : FALSE
130       Parent Id             : e4:5d:37:ff:fe:23:d0:40
131       GMC Id                : 00:00:00:00:00:00:00:01    GMC Class         : 6 (Tx: 6)
132       GMC Accuracy          : 33 (Tx: 33)                GMC Variance      : 20061 (Tx: 20061)
133       GMC Priority1         : 128                        GMC Priority2     : 128 (Tx: 128)
134       Global Data:
135       UTC Offset            : 37                         Leap-59           : FALSE
136       Leap-61               : FALSE                      Time traceable    : TRUE
137       Freq Traceable        : TRUE                       Time Scale        : TRUE
138       Time source           : 160                        Path Trace count  : 0
```

NOTE At the time of writing this book, the ACX710 doesn't support the G.8275.2 profile. This support will come in future releases.

Bi-directional Chain of T-BCs with g.8275.1-profile

Figure 3.10 T-BCs with g.8275.1 profile-Bi-directional Chain



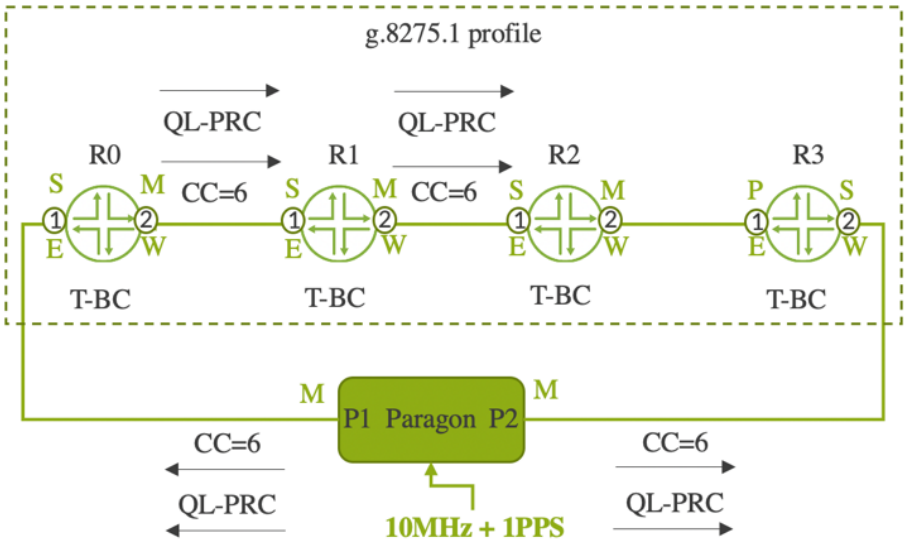
In Figure 3.10, both the P1 and P2 ports of the tester act as a master. Let's assume that all attributes of both masters are the same except the grandmaster clock identity. In this case, ABMCA selects the best master

based on the step removal algorithm. Let's say the GMC-ID of P1 is better than that of P2. In that case, both R0 and R1 locks to P1, whereas R2 and R3 locks to P2. This is not true with the default profile. In the default

profile, devices run BMCA instead of ABMCA and hence all devices select P1. That means with the default profile there is no way that you can make R3 and R2 lock to P2 instead of P1, as R3/R2 are just one to two hops away from P2, respectively. This is a limitation in BMCA and is addressed in the g.8275.1 profile with the ABMC algorithm. Note that the PTP port state of xe-0/0/1 of R2 is indicated as P', which means the port is placed in the *passive* state.

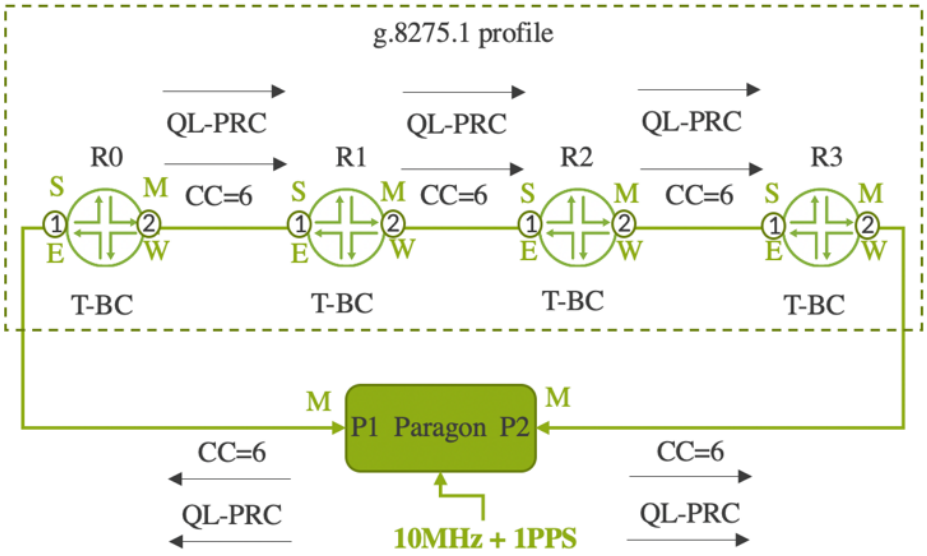
The ITU-T g.8275.1 profile introduced a new attribute called *local priority* in ABMCA. The default value of the local priority is 128. In Junos, it can be configured either per stream or per port. Let's say you configure local priority value 1 to the xe-0/0/1 of R2. In this case, R2 will switch its master from P2 to P1 as illustrated in Figure 3.11.

Figure 3.11 T-BCs with g.8275.1 Profile-Bidirectional Chain Local Priority



Similarly, if you configure local priority value 1 to xe-0/0/1 of R3, even R3 will switch its master from P2 to P1. If you configure a better `priority-2` for the P1 master as compared to that of P2, then all devices will lock to the P1 master, irrespective of the configured local priority. This is illustrated in Figure 3.12.

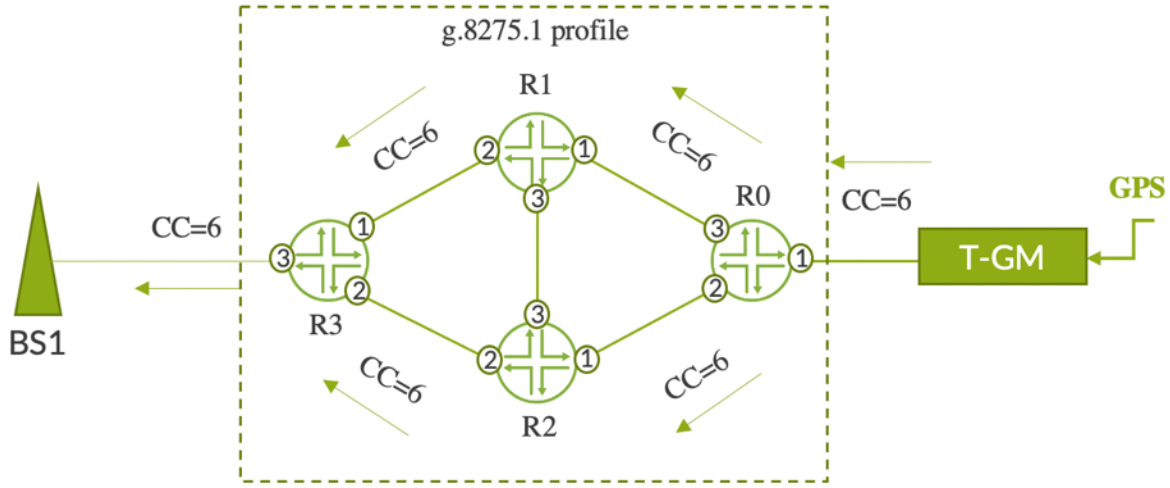
Figure 3.12 T-BCs with g.8275.1 profile-Bidirectional Chain Priority-2



Ring Network of T-BCs with g.8275.1-profile

Let's consider the topology in Figure 3.13, where T-GM is connected to xe-0/0/1 of R0, and BS1 is connected to xe-0/0/3 of R3.

Figure 3.13 T-BCs with g.8275.1 Profile-Ring Network



PTP is configured with stateful ports. Initially xe-0/0/1 of R1 and R2 transitioned to client state and xe-0/0/2 and xe-0/0/3 of R1 and R2 are transitioned to master state. On R3, xe-0/0/1 becomes client and xe-0/0/2 becomes passive.

Let's understand a few failover and local priority configuration scenarios.

Link fail between R1 and R0:

- In this scenario, xe-0/0/3 of R1 transition to client from master state.
- xe-0/0/1 of R3 transition to passive state from client state

- xe-0/0/2 of R3 transition to client state from passive state

Introduce additional link fail between R1 and R2:

- R1 moves to holdover mode.
- xe-0/0/1 of R3 receive CC=135/165 based on holdover state of R2 and moves to master state.
- xe-0/0/2 of R3 continue to be client.

Restore all links. Configure LP=15 on xe-0/0/2 of R2 and LP=30 on xe-0/0/1 of R2:

- xe-0/0/2 of R2 transition to client state and xe-0/0/1 of R2 transition to either master or passive state.

Configure LP=15 on xe-0/0/3 of R1 and LP=20 on xe-0/0/1 of R1:

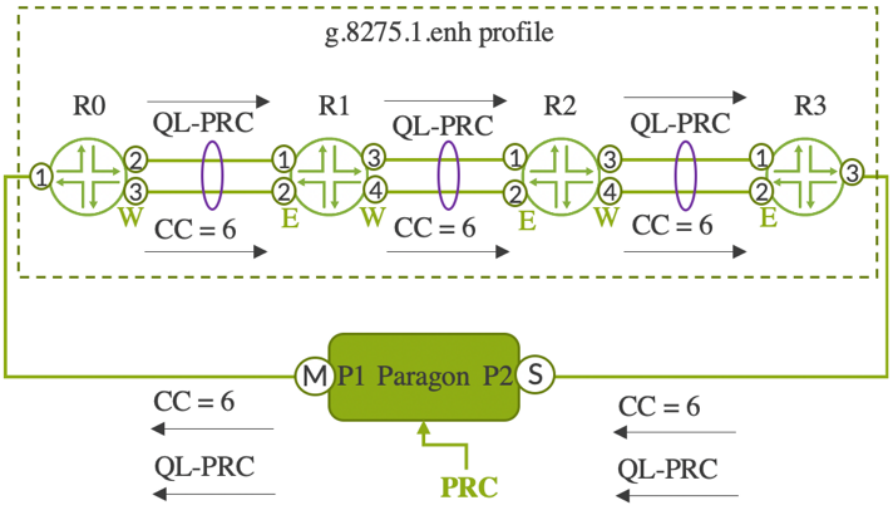
- xe-0/0/3 of R1 transition to client state and xe-0/0/2 of R1 moves to master state. xe-0/0/1 of R3 transition to client state. This forms a timing loop between R1, R2 and R3.

So, one has to use the local priority very carefully to avoid timing loops in G.8275.1-enabled networks. Any misconfiguration of local priority can lead to a permanent timing loop.

PTP over Link Aggregation Group – G.8275.1.enh profile

Figure 3.14 depicts the PTP over Aggregated Ethernet (AE). The Link Aggregation Group (LAG) or AE is formed by the aggregation of two or more member ports. One of the member ports participating in PTP over AE is referred to as primary and other as secondary.

Figure 3.14 T-BCs with g.8275.1.enh Profile-LAG



Care has to be taken to configure the right member ports as primary and secondary between two end points of the LAG bundle. For example, xe-0/0/2 of R0 and xe-0/0/1 of R1 can be configured as primary and the

alternate ports can be configured as secondary. Usually for PTP masters or clients, streams are created on the FPC on which the primary IFL is residing. In the event the primary IFLs are down, then the streams corresponding to secondary IFLs shall be created. Let's look at the configurations on R0 and R1.

NOTE At the time of writing this book, only the MX platform supports PTP over LAG with G.8275.1.enh profile.

Example 3.44 Configuration of g.8275.1.enh profile on R0

```
user@R0# show protocols ptp
clock-mode boundary;
profile-type g.8275.1.enh;
priority2 1;
phy-timestamping;
slave {
    hybrid;
}
stateful {
    interface xe-0/0/1.0 {
        multicast-mode {
            transport {
                ieee-802.3 link-local;
            }
        }
    }
    interface ae0.0 {
        multicast-mode {
            transport {
                ieee-802.3 link-local;
            }
        }
        primary xe-0/0/2;
        secondary xe-0/0/3;
    }
}
```

Example 3.45 Configuration of chassis synchronization on R0

```
user@R0# show chassis
synchronization {
    network-option option-1;
    selection-mode received-quality;
    quality-mode-enable;
    source {
        interfaces xe-0/0/1 {
            priority 1;
            wait-to-restore 0;
            quality-level prc;
        }
    }
    esmc-transmit {
        interfaces all;
    }
}
```

Example 3.46 Configuration of g.8275.1.enh profile on R1

```
user@R1# show protocols ptp
clock-mode boundary;
profile-type g.8275.1;
priority2 2;
phy-timestamping;
slave {
    hybrid;
}
stateful {
    interface ae0.0 {
        multicast-mode {
            transport {
                ieee-802.3 link-local;
            }
        }
        primary xe-0/0/1;
        secondary xe-0/0/2;
    }
    interface ae1.0 {
        multicast-mode {
            transport {
                ieee-802.3 link-local;
            }
        }
        primary xe-0/0/3;
        secondary xe-0/0/4;
    }
}
```

Example 3.47 Configuration of chassis synchronization on R1

```
user@R1# show chassis
synchronization {
    network-option option-1;
    selection-mode received-quality;
    quality-mode-enable;
    source {
        interfaces xe-0/0/1 {
            priority 1;
            wait-to-restore 0;
            aggregated-ether ae0;
            quality-level prc;
        }
        interfaces xe-0/0/2 {
            priority 1;
            wait-to-restore 0;
            aggregated-ether ae0;
            quality-level prc;
        }
    }
    esmc-transmit {
        interfaces all;
    }
}
```

PTP Support for Broadcast Applications-Media Profile

The media profiles can be enabled by specifying the PTP profile-type, smpte', aes67-smpte', and aes67 in the PTP configurations. The media profiles use PTP over IPv4 multicast and include some profile specific options that are summarized in Tables 3.6 through 3.8 earlier in this chapter.

Figure 3.15 T-BCs with Media Profile-Spine-Leaf Architecture

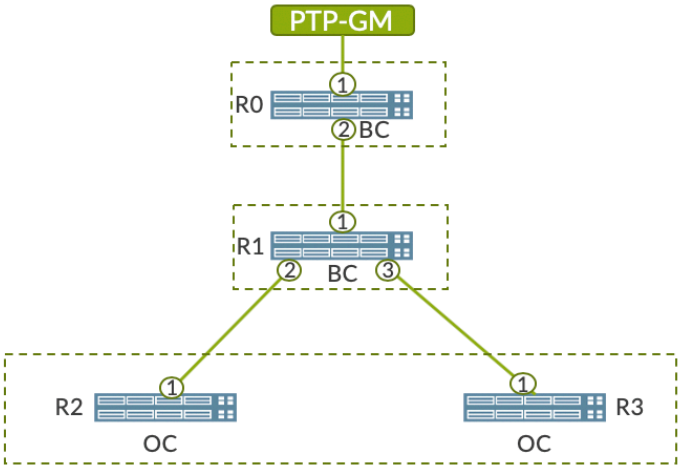


Figure 3.15 depicts the basic spine-leaf architecture of the broadcast network. Usually the endpoints connected to R1 can be a camera or a video switcher, or audio devices. SMPTE and AES67+SMPTE use a PTP management TLV called *SM TLV*. The SM TLV is sent once per second and when master locking status changes. A PTP boundary clock, upon receiving the SM TLV, forwards it in the downstream direction with `boundaryHops` field in SM TLV decremented by 1. The endpoints are really the consumer of this TLV. If no SM TLV is received, then no SM TLV will be forwarded to the remote clients.

A few notes about the media-profile support:

- The SMPTE profile will use the normal PTP DSCP default (value 0xE0). In AES67 profile, PTP announce, sync, and delay request/response packets will use the DSCP value of EF (46), while the media stream will use AF41 (34), and the PTP signaling and management packets will have DF (0). The user can override the DSCP value by using the PTP configuration control `ipv4-dscp`.
- The QFX5220 platform requires the chassis to be placed in `ptp-mode` when the boundary clock is configured. This will disable the et-0/0/32 in QFX5220-32CD, or the et-0/0/128 in QFX5220-128C, and enable the PTP FPGA path. The CLI configuration to do this is `chassis fpc 0 pic 0 ptp-mode`.
- Juniper's platform doesn't support generation of unicast delay-request packets. However, it receives and processes the unicast delay-request packets from remote clients while the port acts as a master.

There are no configuration changes between various PTP media-profiles other than the `profile-type`. There is an additional configuration option for `Delay-request Time-out`. This will help timeout the learned remote clients when the client stops sending delay request packets, after the specified timeout.

Example 3.48 Configuration of smpte Profile on R0

```
user@R0# show protocols ptp
clock-mode boundary;
profile-type smpte;
slave {
    interface xe-0/0/1.0 {
        multicast-mode {
            transport {
                ipv4;
            }
            local-ip-address 1.1.1.1;
        }
    }
}
master {
    interface xe-0/0/2.0 {
        multicast-mode {
            transport {
                ipv4;
            }
            local-ip-address 2.2.2.2;
        }
    }
}
```

Example 3.49 Configuration of smpte Profile on R1

```
user@R1# show protocols ptp
clock-mode boundary;
profile-type smpte;
slave {
    interface xe-0/0/1.0 {
        multicast-mode {
            transport {
                ipv4;
            }
            local-ip-address 2.2.2.1;
        }
    }
}
master {
    interface xe-0/0/2.0 {
        multicast-mode {
            transport {
                ipv4;
            }
            local-ip-address 3.3.3.3;
        }
    }
    interface xe-0/0/3.0 {
        multicast-mode {
            transport {
                ipv4;
            }
            local-ip-address 4.4.4.4;
        }
    }
}
```

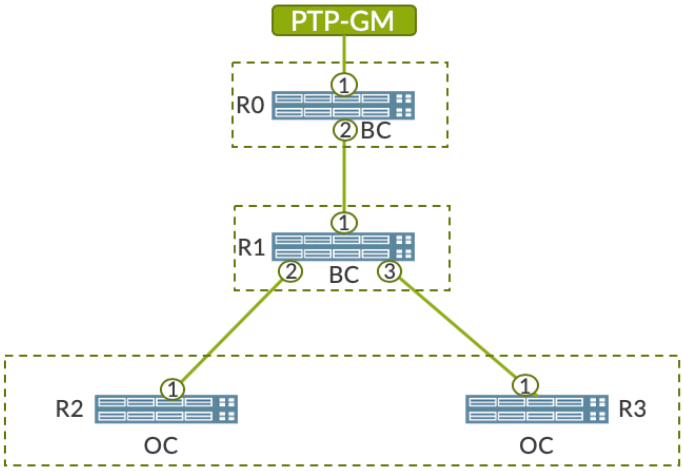
Example 3.49 PTP global information on R0

```
user@R0# run show ptp global-information
PTP Global Configuration:
Domain number           : 127
Clock mode              : Boundary
Profile type            : SMPTE ST-2059-2
Priority Level1         : 128
Priority Level2         : 128
Local Priority          : <not applicable>
Path Trace              : Disabled
Unicast Negotiation     : Disabled
ESMC QL From Clock Class: Disabled
Clock Class/ESMC QL     :  -
SNMP Trap Status        : Disabled
PHY Time Stamping       : Disabled
UTC Leap Seconds        : 37
Transparent-clock-config : DISABLED
Transparent-clock-status : N/A
  Sync Interval         : <not applicable>
  Delay Request Interval: -3 (8 packets per second)
  Announce Interval     : <not applicable>
  Announce Timeout      : 3
  Grant Duration        : <not applicable>
Master Parameters:
  Sync Interval               : -3 (8 packets per second)
  Announce Interval           : -2 (4 packets per second)
  Min Announce Interval       : -3 (8 packets per second)
  Max Announce Interval       : 1 (1 packet every 2 seconds)
  Min Sync Interval           : -7 (128 packets per second)
  Max Sync Interval           : -1 (2 packets per second)
  Min Delay Response Interval : -7 (128 packets per second)
  Max Delay Response Interval : 4 (1 packet every 16 seconds)
  Delay Request Timeout       : 60
  Clock Step                  : one-step
  Arbitrary Mode              : FALSE

Number of Slaves       : 1
Number of Masters      : 1
Number of Stateful     : 0
```

PTP support for Enterprise/Financial Applications-Enterprise Profile

The PTP enterprise profile is used in enterprise and financial markets. This profile helps to time-stamp events on different systems within a large enterprise network with varying latencies and delays (Figure 3.16). It uses PTP over IPv4 and IPv6 multicast communications. Configurations of the enterprise profile are the same as that of the media profile except for the profile type and SM TLV. SM TLV is not used in the enterprise profile.

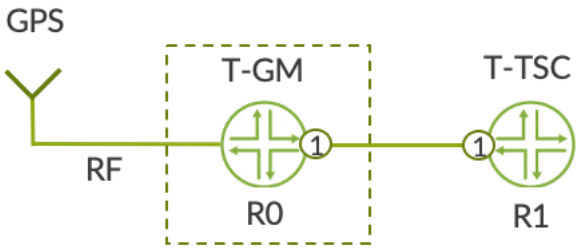
Figure 3.16 T-BCs with Enterprise Profile



T-GM support with Default Profile

The Juniper ACX500 platform supports T-GM functionality with a default profile using PTP transport IEEE-802.3 and IPv4. The ACX500 receives RF input from the GPS Antenna and delivers PTP and SyncE towards the downstream client. Figure 3.17 depicts ACX710 as T-GM delivering clock to T-TSC.

Figure 3.17 T-GM with Default Profile



Let's now look at the configuration on R0 and R1 to enable the T-GM and T-TSC functionality, respectively. Line numbers 2 to 7 in Example 3.50 indicate that the `clock-mode is ordinary` master and the transport is `ieee-802.3`. In the Example 3.51, line number 16, the configured constellation is `gps-and-glonass`. However, you can change the constellation to `gps`, `glonass`, `gps-qzss`, and `gps-qzss-and-glonass`.

Example 3.50 PTP configuration on R0

```
1         user@R0# show protocols ptp
2         clock-mode ordinary;
3         master {
4             interface ge-0/0/1.0 {
5                 multicast-mode {
6                     transport {
7                         ieee-802.3;
8                     }
9                 }
```

```
10          }
11      }
```

Example 3.51 Chassis synchronization configuration on R0

```
12      user@R0# show chassis synchronization
13      network-option option-1;
14      port gnss {
15          client {
16              constellation gps-and-glonass;
17              anti-jamming;
18          }
19      }
20      esmc-transmit {
21          interfaces all;
22      }
```

Example 3.52 PTP configuration on R1

```
23      user@R1# show protocols ptp
24      clock-mode ordinary;
25      master {
26          interface ge-0/0/1.0 {
27              multicast-mode {
28                  transport {
29                      ieee-802.3;
30                  }
31              }
32          }
33      }
```

Example 3.53 Chassis synchronization configuration on R1

```
34      user@R1# show chassis
35      synchronization {
36          network-option option-1;
37          selection-mode received-quality;
38          quality-mode-enable;
39          source {
40              interfaces xe-0/0/1 {
41                  priority 1;
42                  wait-to-restore 0;
43                  quality-level prc;
44              }
45          }
46          esmc-transmit {
47              interfaces all;
48          }
49      }
```

Now let's verify the T-GM lock status, Tx Clock details and GNSS status by issuing the following CLI commands. It is clear that the T-GM is in `PHASE-ALIGNED` state and the Antenna status is `GPS Antenna Good'`.

Example 3.54 PTP lock-status on R0

```
1       user@R0# run show ptp lock-status detail
2       Lock Status:

3       Lock State    : 5 (PHASE ALIGNED)
4       State since   : 2020-09-25 06:46:50 PDT (01:34:50 ago)

5       Source: External GPS/GNSS
```

Example 3.55 PTP clock detail on R0

```
6       user@R0# run show ptp clock detail
7       Clock Details:

8       Slot Number           : 0
9       Default Data:
10      Two-step Clock        : FALSE                      Clock Identity :
0c:86:10:ff:fe:f9:96:80
11      Total Ports on Device : 32                         Clock Class    : 52
12      Clock Accuracy        : 254                        Log Variance   : 15353
13      Clock Priority1       : 128                        Clock Priority2: 128
14      UTC Offset            : 37                         Leap59         : FALSE
15      Leap61                : FALSE                      Time Traceable  : FALSE
16      Frequency Traceable    : FALSE                      Time Source    : 0
17      Delay Req Sending Time: 0                          Steps Removed  : 0
18      Slave-only            : NA
19      Parent Data:
20      Parent Id             : 0c:86:10:ff:fe:f9:96:80
21      GMC Id                : 0c:86:10:ff:fe:f9:96:80   GMC Class        : 6
22      GMC Accuracy          : 33                         GMC Variance     : 15353
23      GMC Priority1         : 128                        GMC Priority2    : 128
24      Global Data:
25      UTC Offset            : 37                         Leap-59          : FALSE
26      Leap-61               : FALSE                      Time traceable    : TRUE
27      Freq Traceable        : TRUE                       Time Scale       : TRUE
28      Time source           : 32
```

Example 3.56 GNSS status on R0

```
29      user@R0# run show chassis synchronization gnss extensive

30      Receiver Status          : Good
31      Constellation            : GPS & GLONASS
32      Cable delay compensation : 0
33      Antenna Status           : GPS Antenna Good
34      Position                 : 12 56' 35.786415'' N   : 77 41' 32.051098'' E
35      Altitude                 : 830 meters
36      Number of satellites     : 14
37      Satellite List:

38      Sat No    Signal Level     Status        Type          Mode(T=Timing/P=Position)
39              40    dBHZ       Acquired      GPS           T,P
40              45    dBHZ       Acquired      GPS           T,P
41              37    dBHZ       Acquired      GPS           T,P
42              42    dBHZ       Acquired      GPS           T,P
43              38    dBHZ       Acquired      GPS           T,P
44              42    dBHZ       Acquired      GPS           T,P
45              45    dBHZ       Acquired      GPS           T,P
46              39    dBHZ       Acquired      GPS           T,P
47              45    dBHZ       Acquired      GPS           T,P
48              45    dBHZ       Acquired      GLONASS       T,P
49              44    dBHZ       Acquired      GLONASS       T,P
50              43    dBHZ       Acquired      GLONASS       T,P
51              43    dBHZ       Acquired      GLONASS       T,P
52              44    dBHZ       Acquired      GLONASS       T,P
```

Basic PTP Troubleshooting Practices

Check all the basic PTP configuration nuances on the router.

- Make sure a proper clock source is used for feeding the clock to the network.
- Make sure the configurations are correct as per the PTP profile. Refer to Chapter 3.
- Know the limitations captured in previous Chapters.

Enable and log all traces related to clock synchronization and verify these logs for any error and anomaly:

```
user@R0# show protocols
clock-synchronization {
    traceoptions {
        file PTP size 1000000;
        flag all;
        flag debug;
    }
}
```

Check PTP Lock Status and verify that the lock status moves to Phase-aligned with no alarm/error:

```
user@R0# run show ptp lock-status detail
Lock Status:

Lock State    : 5 (PHASE ALIGNED)
Phase offset  : 0.000000012 sec
State since   : 2020-09-23 23:53:42 PDT (3d 09:46 ago)

Selected Master Details:
Upstream Master address    : 00:00:00:00:00:00:00:01
Slave interface            : xe-0/1/9.0
Clock reference state      : Clock locked
1pps reference state       : Clock qualified
```

Check hybrid Status and verify that the frequency and phase plane are locked:

```
user@R0# run show ptp hybrid status detail
Hybrid Mode Status:
Configured Mode                : Hybrid
Operating  Mode                : Hybrid
PTP Reference                  : 00:00:00:00:00:00:00:01, xe-0/1/9.0
Synchronous Ethernet Reference : xe-0/1/9
Lock state                     : Locked
Lock state description         : Frequency Locked Phase Locked
```

Check chassis synchronization clock-module. This will tell how long the clock module is in the locked state:

```
user@R0# run show chassis synchronization clock-module
re0:
Clock module on SCB0
  Current role     : master
  Current state    : locked to xe-0/0/1
    State for      : 1 days, 11 hrs, 29 mins, 51 secs
    State since    : Tue Sep  8 09:13:04 2020
  Monitored clock sources
    Interface      Type         Status
    xe-0/0/1       ptp-hybrid   qualified-selected
```

Check the PTP statistics on RE:

```
user@R0# run show ptp statistics detail

Local Clock      Remote Clock       Role  Stream      Received  Transmitted
ae0.0            01:80:c2:00:00:0e Slave       5       5613036      2274551
xe-0/0/1

         Signalling    Announce        Sync       Delay       Error
   Rx:            0     1112860     2225690     2225674           4
   Tx:            0           0           0     2225739           0

Local Clock      Remote Clock       Role  Stream      Received  Transmitted
xe-0/0/2.0       01:1b:19:00:00:00 Master      4             0      3790535
         Signalling    Announce        Sync       Delay       Error
   Rx:            0           0           0           0           0
   Tx:            0     1263518     2527017           0           0
```

Check the PTP stream details on PFE. Streams are identified by `Stream Handle`:

```
SMPC0(R0 vty)# sh clksync ptp streams
PTP all clocks information ..
Local Address    Role   ifl_index  ifl/a_gen  Local DPC  Port Hdl   IFL Hdl
------------------------------------------------------------------------------
38:4f:49:82:d8:5b  stateful      332         141/0         1         2       385
Local Priority : 128
    Stream Handle : 5
        Remote Address       : 1:80:c2:0:0:e     Role: stateful
38:4f:49:82:d8:5e  stateful      333         142/0         1         1       481
Local Priority : 128
    Stream Handle : 4
        Remote Address       : 1:1b:19:0:0:0     Role: stateful
38:4f:49:82:dc:4b  master      337         146/0         1         3       32897
Local Priority : 128
    Stream Handle : 6
        Remote Address       : 1:1b:19:0:0:0     Role: slave
        Slave Type : 0     Slave State: 3
38:4f:49:82:dc:4c  master      338         147/0         1         4       32929
Local Priority : 128
    Stream Handle : 7
        Remote Address       : 1:1b:19:0:0:0     Role: slave
        Slave Type : 0     Slave State: 3
38:4f:49:82:dc:4e  stateful      340         149/0         1         5       32993
Local Priority : 128
    Stream Handle : 8
        Remote Address       : 1:1b:19:0:0:0     Role: stateful
```

Check the PTP statistics on PFE. Identify the stream and check for the statistics per stream:

```
SMPC0(R0 vty)# sh ptp stream 4 statistics
PTP Stream Statistics for   4:
Received:
  Announce           :    7230944 (0 Invalid)
  Sync               :        943 (0 Invalid)
  Follow-Up          :          0 (0 Invalid)
  Delay-Resp         :        939 (0 Invalid)
  Grant-Announce     :          0 (0 Invalid)
  Grant-Sync         :          0 (0 Invalid)
  Grant-Delay-Resp   :          0 (0 Invalid)
  Invalid Domain     :          0
Transmitted:
  Delay-Request      :        944
  Request-Announce   :          0
  Request-Sync       :          0
  Request-Delay_Resp :          0
```

```
Master:
Received:
  Req-Announce_Recv          :          0 (0 Invalid)
  Req-Sync_Recv              :          0 (0 Invalid)
  Request-Delay_Recv         :          0 (0 Invalid)
  Delay_Request_Recv         : 1338410768 (0 Invalid)
  Request-MultiTlv_Recv      :          0 (0 Invalid)
  Request-MultiTlv_Ann_Recv  :          0 (0 Invalid)
  Request-MultiTlv_Sync_Recv :          0 (0 Invalid)
  Request-MultiTlv_Delay_Recv:          0 (0 Invalid)
Transmitted:
  Announce_Sent              :    6033944
  Sync_Sent                  :   12067881
  Grant-Announce_Sent        :          0
  Grant-Sync_Sent            :          0
  Grant-Delay_Sent           :          0
  Delay_Resp_Sent            : 1338410768
  Grant-Multi_Sent           :          0
  Grant-Multi_Ann_Sent       :          0
  Grant-Multi_Sync_Sent      :          0
  Grant-Multi_Delay_Sent     :          0
```

Check the clock ref-info on the client line card in PFE. This will indicate the status of Chassis clock from CB (Ref4 and Ref5), 10MHz clock and 1PPS clock from PTP FPGA to DPLL (Ref7 and Ref9), respectively, and SyncE recovered clock in case of Hybrid (Ref0 and Ref1). For platform which has hardware/software support to keep SyncE and PTP plane independent, SyncE clock recovery happens in CB. So clocksync ref-info doesn't show Ref0 and Ref1 in line card:

```
RMPC0(R0 vty)# sh clksync ref-info
System mode : Centralized
   SCB0 Ref - Ref id 4
      SCM status   : Good
      CFM status   : Good
      GST status   : Good
      PFM status   : Good
   SCB1 Ref - Ref id 5
      SCM status   : Failed
      CFM status   : Failed
      GST status   : Failed
      PFM status   : Failed

PTP reference status ...
 1pps aligned   : TRUE
 PTP fail flag  : 0
 PTP slave      : TRUE
 Interface name : xe-0/1/9
   Fsm state        : Qualified state
   Last event       : Clock qualified
   Reference status : QUALIFIED
   Ref - Ref id 7
      SCM status   : Good
      CFM status   : Good
      GST status   : Good
      PFM status   : Good
   Sync - Ref id 9
      SCM status   : Good
      CFM status   : Good
      GST status   : Good
      PFM status   : Good

SyncE primary reference status ...
 Interface name : xe-0/1/9
```

```
   Fsm state        : Qualified state
   Last event       : Clock qualified lock
   Reference status : QUALIFIED
   Pri - Ref id 0
      SCM status    : Good
      CFM status    : Good
      GST status    : Good
      PFM status    : Good

SyncE secondary reference status ...
 Interface name :
   Fsm state        : Init state
   Last event       : No clock
   Reference status : MONITORING
   Sec - Ref id 1
      SCM status    : Failed
      CFM status    : Failed
      GST status    : Failed
      PFM status    : Failed
Intr rx count: 0
```

Check the clock dpll-info on the Client line card. This will indicate the status of DPLL-2 (Ref7 and Ref8) on the Client line card:

```
RMPC0(R0 vty)# sh clksync dpll-info

DPLL-1 Configuration ...
   Mode                 : Forced reference-lock
   Selected Reference   : 4

DPLL-1 Status....
   Lock Status      : Locked
   Lost Lock Status : False
   Holdover Status  : False

DPLL-2 Configuration ...
   Mode                 : Forced reference-lock
   Selected Reference   : 7

DPLL-2 Status....
   Lock Status      : Locked
   Lost Lock Status : False
   Holdover Status  : False

DPLL-3 Configuration ...
   Mode                 : Forced reference-lock
   Selected Reference   : 2

DPLL-3 Status....
   Lock Status      : Unlocked
   Lost Lock Status : False
   Holdover Status  : False

DPLL-4 Configuration ...
   Mode                 : Forced reference-lock
   Selected Reference   : 0

DPLL-4 Status....
   Lock Status      : Locked
   Lost Lock Status : False
   Holdover Status  : False
```

Check the clock ref-info on the Master line card. This will indicate the status of Chassis clock from CB (Ref4 and Ref5) and the status on 1PPS and 10MHz clock to DPLL (Ref2 and Ref3):

```
SMPC6(R0 vty)# sh clksync ref-info

System mode : Centralized
   SCB0 Ref - Ref id 4
      SCM status   : Good
      CFM status   : Good
      GST status   : Good
      PFM status   : Good
   SCB1 Ref - Ref id 5
      SCM status   : Failed
      CFM status   : Failed
      GST status   : Failed
      PFM status   : Failed

PTP reference status ...
 1pps aligned   : TRUE
 PTP fail flag  : 0
 PTP slave      : FALSE
 Interface name : xe-0/1/9
   Fsm state        : Qualified state
   Last event       : Clock qualified
   Reference status : QUALIFIED
   Ref - Ref id 2
      SCM status   : Good
      CFM status   : Good
      GST status   : Good
      PFM status   : Good
   Sync - Ref id 3
      SCM status   : Good
      CFM status   : Good
      GST status   : Good
      PFM status   : Good
Intr rx count: 0
```

Check the clock dpll-info on the Master line card. This will indicate the status of DPLL-3 (Ref2 and Ref3) on the Master line card:

```
SMPC6(R0 vty)# sh clksync dpll-info
DPLL-1 Configuration ...
   Mode                 : Forced reference-lock
   Selected Reference   : 4

DPLL-1 Status....
   Lock Status      : Locked
   Lost Lock Status : False
   Holdover Status  : False

DPLL-2 Configuration ...
   Mode                 : Forced reference-lock
   Selected Reference   : 7

DPLL-2 Status....
   Lock Status      : Unlocked
   Lost Lock Status : False
   Holdover Status  : False

DPLL-3 Configuration ...
   Mode                 : Forced reference-lock
   Selected Reference   : 2

DPLL-3 Status....
   Lock Status      : Locked
   Lost Lock Status : False
   Holdover Status  : False
```

```
DPLL-4 Configuration ...
   Mode                 : Forced reference-lock
   Selected Reference   : 0
DPLL-4 Status....
   Lock Status      : Unlocked
   Lost Lock Status : False
   Holdover Status  : False
```

Check the ptp `nbr-upd-info` on the Client line card. This will indicate the status of `Active PFEs` and `Synced PFEs`:

```
RMPC0(R0 vty)# sh clksync ptp nbr-upd-info

PTP Neighbor info :
====================================
Active PFEs  : 0x0050
Synced PFEs  : 0x0050
Pending PFEs : 0x0000
Sequence No. : 0x01
PTP slave    : Yes
UTC time     : 1601223005 sec 202248191 nsec
Last neighbor update time : 1600931039 sec 64881343 nsec

PTP TOD Statistics :
====================================
    Slave :
        Request Transmitted       : 43
        Request Transmit Failed   : 0
        Response Received         : 2
        Response Reception Failed : 0
        Success Transmitted      : 2
        Success Transmit Failed  : 0
        Sync Received             : 0
        Sync Reception Failed     : 0
        Response Reception Delayed: 0
        Update Retransmission     : 0
    Master:
        Request Received          : 0
        Request Reception Failed  : 0
        Response Transmitted          : 0
        Response Transmit Failed      : 0
        Success Received          : 0
        Success Transmit Failed      : 0
        Sync Transmitted          : 0
        Sync Transmit Failed      : 0
        Update Prior Alignment    : 0
    Timer Status:
        PTP NBR update timer      : 0
        PTP NBR TOD set timer     : 0
        PTP NBR sync msg timer    : 0
        PTP NBR resp msg timer    : 0
```

Check the ptp `nbr-upd-info` on the Master line card. This will indicate the status of `Active PFEs`, `Synced PFEs` and the TOD statistics on Master line card:

```
SMPC6(R0 vty)# sh clksync ptp nbr-upd-info

PTP Neighbor info :
====================================
Active PFEs  : 0x0011
Synced PFEs  : 0x0000
Pending PFEs : 0x0000
Sequence No. : 0x00
PTP slave    : No
UTC time     : 1601222947 sec 58538443 nsec
Last neighbor update time : 1600931039 sec 64881343 nsec
```

```
Last SYNC check transmit time   : 0 sec 0 nsec
Last SYNC check arrival time    : 0 sec 0 nsec
Last SYNC check difference time : 0 sec 0 nsec

PTP TOD Statistics :
====================================
    Slave :
        Request Transmitted       : 0
        Request Transmit Failed   : 0
        Response Received         : 0
        Response Reception Failed : 0
        Success Transmitted      : 0
        Success Transmit Failed  : 0
        Sync Received             : 0
        Sync Reception Failed     : 0
        Response Reception Delayed: 0
        Update Retransmission     : 0
    Master:
        Request Received          : 86
        Request Reception Failed  : 0
        Response Transmitted          : 1
        Response Transmit Failed      : 0
        Success Received          : 1
        Success Transmit Failed      : 0
        Sync Transmitted          : 0
        Sync Transmit Failed      : 0
        Update Prior Alignment    : 84
    Timer Status:
        PTP NBR update timer      : 0
        PTP NBR TOD set timer     : 0
        PTP NBR sync msg timer    : 0
        PTP NBR resp msg timer    : 0
```

Check the PDV data on the Client line card. This will indicate the T1, T2 time-stamp and the correction-field value. You can look for the consistency in CF values:

```
RMPC0(R0 vty)# sh ptp pdv-data 10
  : T1(sec)      T1(nsec)    T2(sec)      T2(nsec)    Seq id  CF
S : 1599806063   743888655   1599806063   743901765   65244   10059
D : 1599806063   689890166   1599806063   689903870   38219   10665
S : 1599806063   681388655   1599806063   681401781   65243   10075
D : 1599806063   629879542   1599806063   629893210   38218   10627
S : 1599806063   618888655   1599806063   618901797   65242   10091
D : 1599806063   564880566   1599806063   564894245   38217   10646
S : 1599806063   556388655   1599806063   556401765   65241   10059
D : 1599806063   504879222   1599806063   504892920   38216   10659
S : 1599806063   493888655   1599806063   493901797   65240   10091
D : 1599806063   439879302   1599806063   439892990   38215   10656
  : T1(sec)      T1(nsec)    T2(sec)      T2(nsec)    Seq id  CF
```

Check state of phydriver_pic_info. SyncState should be SYNC and Valid:

```
RMPC0(R0 vty)# sh clksync phydriver pic_info

PHY driver bitmap: 0x00000000 GlobalSyncState: TRUE MasterState: External

No  MIC PIC  SyncState      MasterStatus PhyCount   SyncState
--  --- ---  ---------      ------------ --------   ---------
 0  0    0   SYNC                None      12       Valid
 1  0    1   SYNC                None      12       Valid
```

Check state of `phydriver_pic_state`. State should be SYNCED.

```
RMPC0(R0 vty)# sh clksync phydriver pic_state 0

FSM Entry: 1 Valid:Yes   PhyCount: 12 State: SYNC

Phy    Valid    State               SyncError   VerifyFailCnt Failures  Tolerance
---    -----    -----               ---------   ------------- --------  ---------
 1     Valid   SYNCED                      0       1             0     50
 2     Valid   SYNCED                      0       1             0     50
 3     Valid   SYNCED                      0       1             0     50
 4     Valid   SYNCED                      0       1             0     50
 5     Valid   SYNCED                      2       1             0     50
 6     Valid   SYNCED                      1       1             0     50
 7     Valid   SYNCED                      0       1             0     50
 8     Valid   SYNCED                      0       1             0     50
 9     Valid   SYNCED                      1       1             0     50
10     Valid   SYNCED                      1       1             0     50
11     Valid   SYNCED                      1       1             0     50
12     Valid   SYNCED                      1       1             0     50
```

Check the PTP servo state of the Client line card. State should be `Phase Aligned`:

```
RMPC0(R0 vty)# sh ptp servo
PTP Servo State:
----------------
Instances: 1, State: Phase Aligned (5)
Freq Offset: 75, Phase Offset: +0.000000009 seconds
DAC Value: 132958, OOR: 0
Uptime: 1599807690, Time Constant: 32, Traffic State: 2
Network: True, FreqInput: True, PhaseInput: False, PDV: False, Hybrid: True
Master->Slave: +0.000003044/+0.000003050/+0.000003052 (min/mean/max sec)
Slave->Master: +0.000003026/+0.000003037/+0.000003044 (min/mean/max sec)
Master->Slave: +0.000000016/+0.000000058/+0.000000128 (Jitter min/mean/max sec)
Slave->Master: +0.000000000/+0.000000071/+0.000000187 (Jitter min/mean/max sec)
```

Check the PTP servo state of the Master line card. State should be `Phase Aligned` and `PhaseInput` is `True`:

```
SMPC6(R0 vty)# sh ptp servo
PTP Servo State:
----------------
Instances: 0, State: Phase Aligned (5)
Freq Offset: 0, Phase Offset: +0.000000000 seconds
DAC Value: 132958, OOR: 0
Uptime: 0, Time Constant: 0, Traffic State: 0
Network: False, FreqInput: False, PhaseInput: True, PDV: False, Hybrid: False
Master->Slave: +0.000000000/+0.000000000/+0.000000000 (min/mean/max sec)
Slave->Master: +0.000000000/+0.000000000/+0.000000000 (min/mean/max sec)
Master->Slave: +0.000000000/+0.000000000/+0.000000000 (Jitter min/mean/max sec)
Slave->Master: +0.000000000/+0.000000000/+0.000000000 (Jitter min/mean/max sec)
```

PTP Support on Juniper Platform/Line Cards

At the time of the writing of this book, PTP is supported on the following platform/line cards:

- The Juniper MX Series supports IEEE Default profile starting MPCEX (X=1 to 2, 4, 5, to 9), NG-MPCE2/3, MX80-P, MX104, MX204, and MX10003.
- The Juniper MX Series supports g.8275.1 starting MPCEX (X=5 to 9), NG-MPCE2/3, MX104, MX204, MX10003, and MX10K-LC2101.
- The Juniper MX Series supports g.8275.1.enh starting MPCEX (X=5 to 9), NG-MPCE2/3, MX104, MX204, and MX10003.
- The Juniper MX Series supports PTP over Ethernet LAG starting MPCEX (X=5 to 9).
- The Juniper MX Series supports PTP over IPv4 LAG starting MPCEX (X=5 to 9), NG-MPCE2/3, MX104, MX204, and MX10003.
- The Juniper MX Series supports T-BC/T-TSC starting MPCEX (X=5 to 9), NG-MPCE2/3, MX104, MX204, and MX10003.
- The Juniper ACX710 supports G.8275.1 profile and Virtual port functionality.
- The Juniper ACX5448-D, ACX5448-M, ACX2X00 (X=1 and 2), ACX1X00 (X=0 and 1), and ACX4000, support IEEE Default profile.
- The Juniper ACX1100 platform supports Enterprise profile.
- The Juniper QFX5110-48s/QFX5200-32c Series supports G.8275.2 IPv4/IPv6, G.8275.2 over AE, and Loopback Interface.
- The Juniper QFX5110-48s/QFX5200-32c supports T-BC-P/T-TSC-P.
- The Juniper QFX5110-48s/QFX5200-32c supports PTP over IPv4 and IPv6 LAG unicast/multicast.
- The Juniper QFX5110-48s/QFX5200-32c/QFX10002 (10G port) supports PTP Media Profile (SMPTE, AES67, AES67+SMPTE).
- The Juniper QFX5220-32CD/QFX10002 (10G port) supports Enterprise Profile.

Summary

This chapter discussed the PTP clock types, PTP packet format, and PTP clock synchronization. State machine explaining various servo state was discussed, as well as various PTP profiles and their attributes compared to the ITU-T standard recommendations. Configurations and verifications of supported PTP profiles for linear, bi-directional, and ring topologies covering various failover scenarios, as well as local clock status and the content of announce messages during various servo states were discussed. Also discussed the basic PTP troubleshooting practices. Finally, various Juniper platforms and line cards that support PTP were listed.

Chapter 4

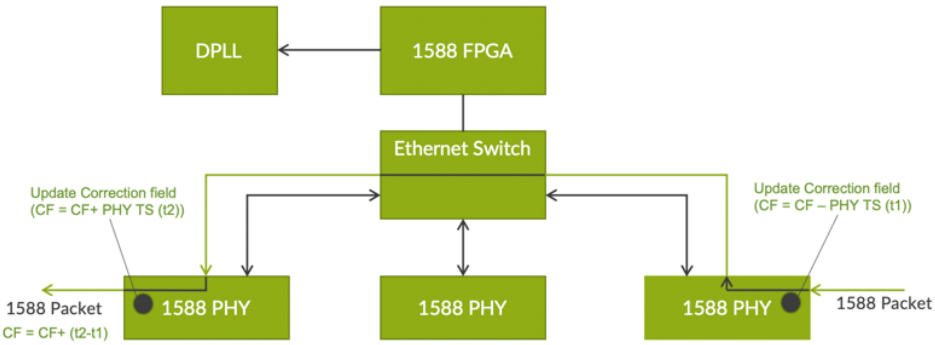
Transparent Clock

Transparent clocks measure the resident delay of the PTP packets inside a device as the packets pass through it. The major portion of the delay experienced by those packets primarily arises from the queuing or buffering delays. Those delays are mainly a function of network load and device architecture, and are the main source of PDV inside the device. The computation of the delay is carried out using the correction field (CF) in the PTP header. The client or boundary clocks can determine this resident time while they receive the PTP packet from the upstream TC device or devices and can estimate and remove these delays from the offset computation and reduce the packet's jitter effects.

The accuracy of the TC depends on the accuracy with which the CF value is updated, while the inaccuracy will depend on the transmission rate and the packet size. Juniper products support timestamping either at the PHY or MAC to compensate for any PDV introduced by the packet processing path of the router/switch. It has been observed that the accuracy is better if the correction is applied at the PHY level. However, in cases where PHY level timestamping is not supported on certain platforms, the correction is performed at the MAC or ASIC level. Figure 4.1 illustrates a scenario where PHY level correction is performed:

- At the ingress, subtract the timestamp from the correction field;
- At the egress, add timestamp to the correction field.

Figure 4.1 TC Timestamping at PHY Level



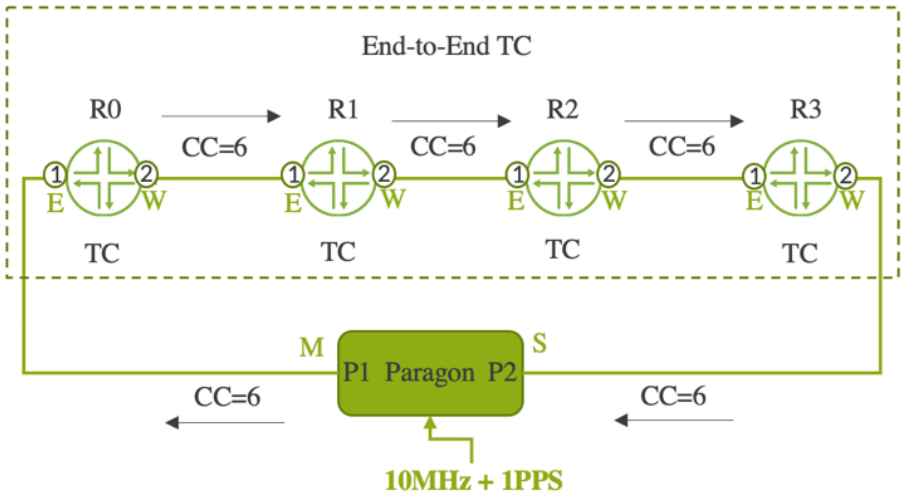
In case of MAC- or ASIC-level timestamping, the internal delays up to the ASIC are compensated manually. These values should be carefully estimated for each port's speed and compensated manually.

Configuring and Verifying TC

End-to-End Transparent Clock - Non-syntonized TC

In Figure 4.2, all the devices are configured as `e2e-transparent` clocks. The tester port P1 acts as master and P2 acts as client.

Figure 4.2 End-to-End Transparent Clock-Non-syntonized TC



Each PTP packet is timestamped by the TC on ingress and egress and the TC estimates the resident delay within the devices and update this value in the correction field (CF) within the PTP packet header. Resident time is the time the PTP packet spends inside the device while it is passing through the router or switch. The downstream client or boundary clock will estimate these variable delays from the CF field and remove these delays while establishing the phase offset to reduce the packet's jitter effect. Configuration of the TC is pretty simple as you'll see in Example 4.1. Once the configuration is applied it gets enabled for all configured physical interfaces on the device. It is important to note that T-BC and TC configurations can't be enabled simultaneously.

Example 4.1 Configuration of End-to-end TC on R0

```
1       user@R0# show protocols ptp
2       e2e-transparent;
```

And let's verify the TC configuration status using the following command. It should show `ENABLED and ACTIVE`.

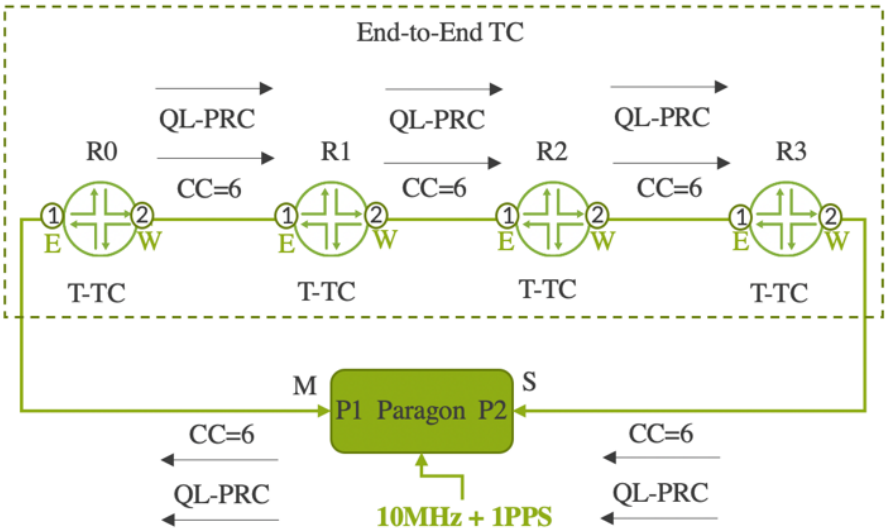
Example 4.2 Verification of End-to-end TC on R0

```
1       user@R0# run show ptp global-information
2       PTP Global Configuration:
3       Transparent-clock-config : ENABLED
4       Transparent-clock-status : ACTIVE
```

End-to-End Telecom Transparent Clock - Syntonized TC

Syntonized TC (Figure 4.3) is standardized in ITU-T G.8273.3 recommendation. It is also called Telecom TC (T-TC).

Figure 4.3 End-to-End Syntonized Transparent Clock



In syntonized TC, the TC requires physical layer frequency based on the ITU-T G.8262/.1 recommendation. Typically, SyncE is recovered from the physical layer and TC uses this recovered clock to generate TOD signals for synchronizing the PTP timestamp counter. It is important to note that SyncE configuration is mandatory for enabling syntonized TC.

Example 4.3 Configuration of Syntonized TC on R0

```
user@R0# show protocols ptp
syntonized-e2e-transparent;
```

Example 4.4 Configuration of chassis synchronization on R0

```
user@R0# show chassis synchronization
network-option option-1;
selection-mode received-quality;
quality-mode-enable;
source {
    interfaces xe-0/0/1 {
        wait-to-restore 0;
        quality-level prc;
    }
}
esmc-transmit {
    interfaces all;
}
```

Let's verify the TC configuration status using the following command. It should show `ENABLED and ACTIVE`. You should also check SyncE status to confirm the clock status as `Locked`.

Example 4.5 Verification of syntonized TC on R0

```
user@R0# run show ptp global-information
PTP Global Configuration:
Syntonized-transparent-clock-config : ENABLED
Syntonized-transparent-clock-status : ACTIVE
```

Example 4.6 Configuration of chassis synchronization on R0

```
user@R0# run show chassis synchronization extensive
Current clock status  : Locked
Clock locked to       : Primary
SNMP trap status      : Disabled

Configured sources:

Interface           : xe-0/0/1
Status              : Primary       Index       : 145
Clock source state  : Clk qualified Priority    : Default(8)
Configured QL       : PRC           ESMC QL     : PRC
Clock source type   : ifd           Clock Event : Clock locked
Wait-to-restore     : 0  min        Hold-off    : 1000 ms
Interface State     : Up,pri,ESMC Rx(SSM 0x2),ESMC TX(QL DNU/SSM 0xf),
```

NOTE At the time of the writing of this book, the Juniper platform doesn't support syntonized TC. However, the syntonized TC feature is planned on the ACX7100-32C and ACX7100-48L in the upcoming release.

TC Support on Juniper Platforms

At the time of the writing of this book, Transparent Clock (TC) is supported on the following platforms:

- The Juniper ACX Series supports Transparent Clock functionality starting with ACX5048, ACX5096, ACX5448-M and ACX5448-D, ACX6360, ACX7100-32C and ACX7100-48L.
- The Juniper ACX Series supports Syntonized Transparent Clock functionality starting ACX7100-32C and ACX7100-48L (Upcoming release)
- The Juniper QFX Series supports Transparent Clock on the following platforms: QFX5100, QFX5110-48S, QFX5110-32Q, QFX5120-48Y, QFX5120-48T, QFX5200-32C, QFX5220-32CD, QFX5220-128C, and QFX10002.

Summary

This chapter provided an overview of Transparent Clock functionality as well as the configuration and verification for 1588 TC and syntonized TC. A summary of various Juniper hardware devices was also listed that support TC features.

Chapter 5

Deploying Synchronization

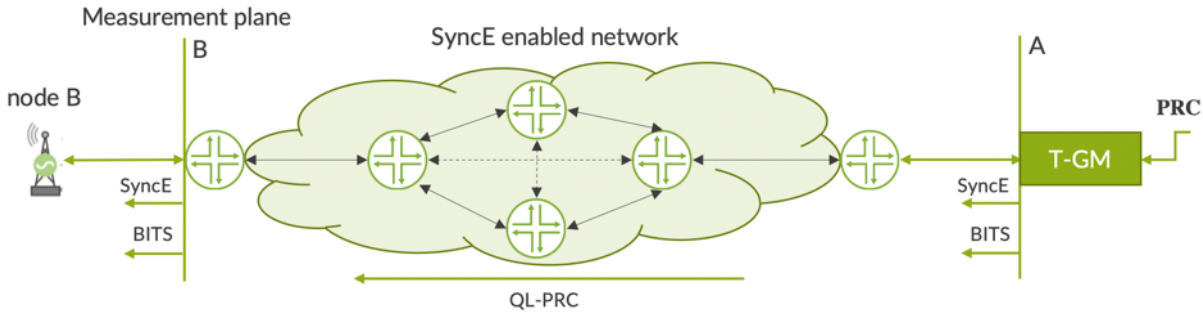
Synchronization deployment plays a prominent role in the next generation of networks. To realize the full potential of 4G/5G networks, highly accurate and precise time synchronization is needed on almost every part of a transport network. These transport networks help distribute the time to the Radio Access Network (RAN). Synchronization requirements vary based on the radio technology and the spectrum used, therefore it is very important for a transport network to meet these challenging requirements. This chapter covers the various timing deployments in a transport network.

End-to-End Synchronous Ethernet Deployment

Readers who are using their network for frequency delivery may deploy SyncE on all devices in the network. The requirement here is to meet the network-wide frequency accuracy set out by ITU-T G.8261 for frequency-only applications. In mobile backhaul deployments this means frequency delivery of 16 parts per billion (ppb) of accuracy to the base station with respect to a stable reference clock. This would help achieve the base station radio interface accuracy requirement of 50ppb.

In end-to-end SyncE deployment the accuracy of the clock doesn't have any bearing on the network load and the network designer must ensure that all the devices in the network must be SyncE capable. If any device in the chain is not SyncE capable or if it is a legacy device that doesn't support SyncE, then the synchronous chain will break, and frequency delivery is not possible by means of SyncE. It's also important to keep in mind that the accuracy of the clock delivered to the base station depends mainly on the onboard oscillator quality and the PLL noise filtering capability on individual nodes. As discussed in an earlier chapter, the ESMC packets that are transmitted by each node ensure the end-to-end traceability of the clock and avoid timing loops. Also, the network should be carefully designed to enable clock propagation via alternate paths in the event of network failure. Figure 5.1 depicts the frequency delivery via SyncE.

Figure 5.1 End-to-End SyncE Deployment

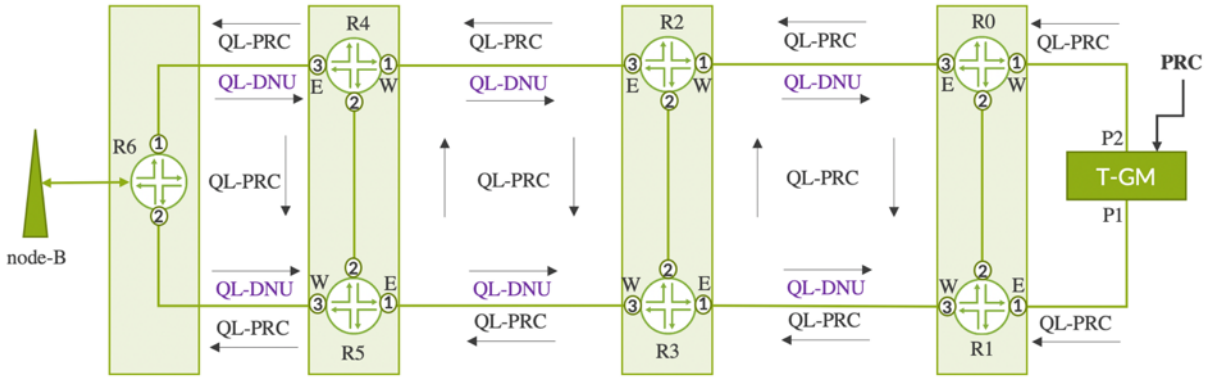


The network input and output can be either SyncE or BITS. T-GM or any stable clock source provide the necessary SyncE or BITS clock to the network. Refer to the section G.8261 Performance Limit in Chapter 6 for details on performance metrics. The network level accuracy requirement is indicated in Table 5.1.

Table 5.1 Network Accuracy Requirement

Network Input	Network Output	Frequency Accuracy	Phase Accuracy
SyncE/BITS (E1/T1)	**SyncE**	**16PPB / As per G.8261**	**NA**
	BITS (E1/T1)	**16PPB / As per G.823**	**NA**

Figure 5.2 End-to-End SyncE Deployment-topology



The configuration details on devices R0 through R6 are furnished in Example 5.1-5.7 below.

Example 5.1 Configuration of chassis synchronization on R0

```
1         user@R0# show chassis
2         network-services enhanced-ip;
3         synchronization {
4             network-option option-1;
5             selection-mode received-quality;
6             quality-mode-enable;
7             source {
8                 interfaces xe-0/0/1 {
```

```
9                   priority 1;
10                  wait-to-restore 0;
11                  quality-level prc;
12              }
13              interfaces xe-0/0/2 {
14                  priority 2;
15                  wait-to-restore 0;
16                  quality-level prc;
17              }
18          }
19          esmc-transmit {
20              interfaces all;
21          }
22      }
```

Example 5.2 Configuration of chassis synchronization on R1

```
23      user@R1# show chassis
24      network-services enhanced-ip;
25      synchronization {
26          network-option option-1;
27          selection-mode received-quality;
28          quality-mode-enable;
29          source {
30              interfaces xe-0/0/1 {
31                  priority 1;
32                  wait-to-restore 0;
33                  quality-level prc;
34              }
35              interfaces xe-0/0/2 {
36                  priority 2;
37                  wait-to-restore 0;
38                  quality-level prc;
39              }
40          }
41          esmc-transmit {
42              interfaces all;
43          }
44      }
```

Example 5.3 Configuration of chassis synchronization on R2

```
45      user@R2# show chassis
46      network-services enhanced-ip;
47      synchronization {
48          network-option option-1;
49          selection-mode received-quality;
50          quality-mode-enable;
51          source {
52              interfaces xe-0/0/1 {
53                  priority 1;
54                  wait-to-restore 0;
55                  quality-level prc;
56              }
57              interfaces xe-0/0/2 {
58                  priority 2;
59                  wait-to-restore 0;
60                  quality-level prc;
61              }
62          }
63          esmc-transmit {
64              interfaces all;
65          }
66      }
```

Example 5.4 Configuration of chassis synchronization on R3

```
user@R3# show chassis
synchronization {
    network-option option-1;
    selection-mode received-quality;
    quality-mode-enable;
    source {
        interfaces xe-0/0/1 {
            priority 1;
            wait-to-restore 0;
            quality-level prc;
        }
        interfaces xe-0/0/2 {
            priority 2;
            wait-to-restore 0;
            quality-level prc;
        }
    }
    esmc-transmit {
        interfaces all;
    }
}
```

Example 5.5 Configuration of chassis synchronization on R4

```
user@R4# show chassis
synchronization {
    network-option option-1;
    selection-mode received-quality;
    quality-mode-enable;
    source {
        interfaces xe-0/0/1 {
            priority 1;
            wait-to-restore 0;
            quality-level prc;
        }
        interfaces xe-0/0/2 {
            priority 2;
            wait-to-restore 0;
            quality-level prc;
        }
    }
    esmc-transmit {
        interfaces all;
    }
}
```

Example 5.6 Configuration of chassis synchronization on R5

```
user@R5# show chassis
network-services enhanced-ip;
synchronization {
    network-option option-1;
    selection-mode received-quality;
    quality-mode-enable;
    source {
        interfaces xe-0/0/1 {
            priority 1;
            wait-to-restore 0;
            quality-level prc;
        }
        interfaces xe-0/0/2 {
            priority 2;
            wait-to-restore 0;
            quality-level prc;
        }
```

```
126          }
127          esmc-transmit {
128              interfaces all;
129          }
130      }
```

Example 5.7 Configuration of chassis synchronization on R6

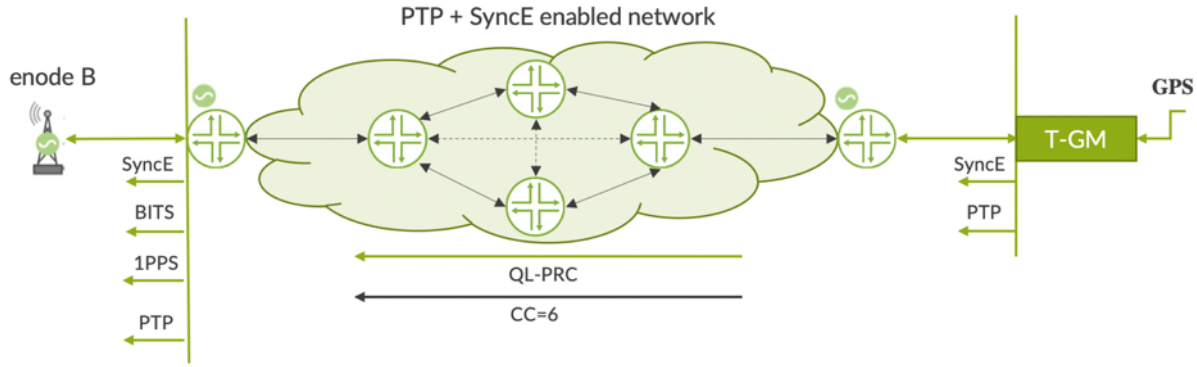
```
131      user@R6# show chassis
132      network-services enhanced-ip;
133      synchronization {
134          network-option option-1;
135          selection-mode received-quality;
136          clock-mode auto-select;
137          quality-mode-enable;
138          interfaces bits {
139              signal-type e1;
140              e1-options {
141                  framing g704;
142              }
143          }
144          output {
145              interfaces bits {
146                  wander-filter-disable;
147                  source-mode chassis;
148                  minimum-quality sec;
149              }
150          }
151          source {
152              interfaces xe-0/0/1 {
153                  priority 1;
154                  wait-to-restore 0;
155                  quality-level prc;
156              }
157              interfaces xe-0/0/2 {
158                  priority 2;
159                  wait-to-restore 0;
160                  quality-level prc;
161              }
162          }
163          esmc-transmit {
164              interfaces all;
165          }
166      }
```

End-to-End G.8275.1 Profile with Full On-path Support

In the phase-profile, networks can be full timing aware or partial timing aware. The ITU-T G.8275.1 profile is defined to operate in full on-path networks, where all the devices are PTP-aware and configured in hybrid mode. That means both PTP and SyncE are configured on all devices with profile type as G.8275.1. The network could be a mix of Layer 2 and Layer 3 devices such as Layer 2 switches and IP/MPLS routers. Typically, the access segment is more about Layer 2 solutions, whereas Layer 3 or IP/MPLS solutions are more often used in the backbone.

NOTE Juniper devices also support the G.8275.1.enh profile, which will additionally support PTP over IPv4 transport and VLAN configurations. However, at the time of writing this book, stateful port is not supported with devices operating in G.8275.1.enh profile (IPv4). Check for updates.

Figure 5.3 End-to-End Hybrid Deployment



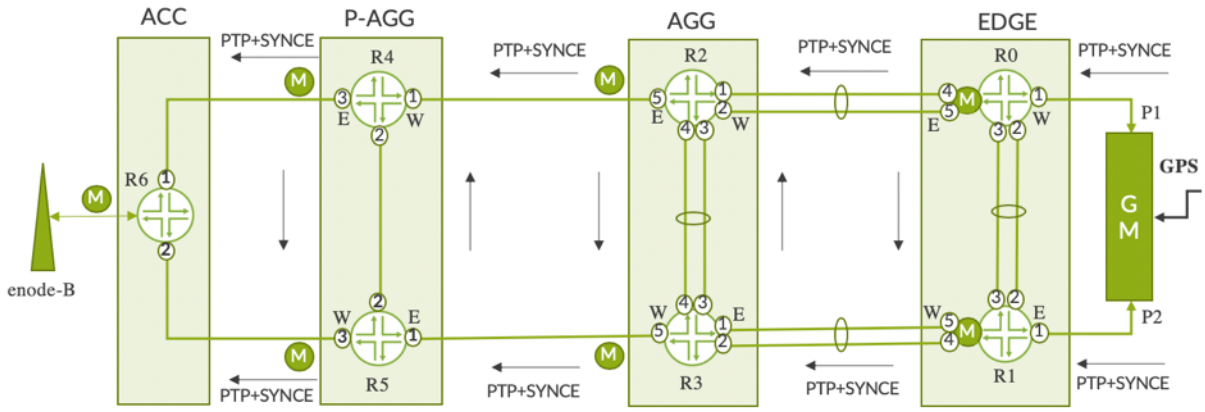
You can see in Figure 5.3 that the Telecom-Grandmaster (T-GM) provides the PTP and SyncE clock to the network and the remote cell site router will recover the clock and deliver frequency, via SyncE or BITS, and phase, via 1PPS or PTP, to the enode B. The network phase requirement is 1100 nsec. Considering the tolerance on the base station budgeting, this means that the phase requirement at the air-interface is 1500 nsec. Refer the section G.8261 Performance Limit and G.8271.1 Performance Limit in Chapter 6 for details on performance metrics. Table 5.2 lists these network wide frequency and phase requirements.

Table 5.2 Network Requirements-on-path Support

Network Input	Network Output	Frequency Accuracy	Phase Accuracy
PTP + SyncE	**SyncE**	**16 PPB / As per G.8261**	**NA**
	BITS	**16 PPB / As per G.823**	**NA**
	1PPS	**NA**	**1100 nsec as per G.8271.1**
	PTP	**16 PPB / As per G.8261.1**	**1100 nsec as per G.8271.1**

In the deployment-topology shown in Figure 5.4, you can see a mix of master-only or explicit master port and stateful ports.

Figure 5.4 End-to-End Hybrid Deployment-topology



The ITU-T G.8275.1 profile permits stateful and master-only configurations. Explicit master was chosen on those ports because a proper synchronization design must ensure upstream nodes don't recover clock from downstream nodes. Even with stateful ports configured throughout the network, there isn't any anticipation of clock loops; it is a best practice precaution, however.

For each Aggregated Ethernet (AE) IFL configured as a PTP client or master, you can designate one member IFL as primary and another as secondary. In hybrid mode PTP over LAG, the primary and secondary interfaces must reside on the same line card. The configured port states of various ports are summarized in Table 5.3.

Table 5.3 Ports Operating Mode

Nodes	Port	Member	Port role
R0	xe-0/0/1	NA	Stateful
	ae0	xe-0/0/2(Primary) xe-0/0/3(Secondary)	Stateful
	ae1	xe-0/0/4(Primary) xe-0/0/5(Secondary)	Master
R1	xe-0/0/1	NA	Stateful
	ae0	xe-0/0/2(Primary) xe-0/0/3(Secondary)	Stateful
	ae1	xe-0/0/4(Primary) xe-0/0/5(Secondary)	Master
R2	ae0	xe-0/0/1(Primary) xe-0/0/2(Secondary)	Stateful
	ae1	xe-0/0/3(Primary) xe-0/0/4(Secondary)	Stateful
	xe-0/0/5	NA	Master
R3	ae0	xe-0/0/1(Primary) xe-0/0/2(Secondary)	Stateful

	ae1	xe-0/0/3(Primary) xe-0/0/4(Secondary)	Stateful
	xe-0/0/5	NA	Master
R4	xe-0/0/1	NA	Stateful
	xe-0/0/2	NA	Stateful
	xe-0/0/3	NA	Master
R5	xe-0/0/1	NA	Stateful
	xe-0/0/2	NA	Stateful
	xe-0/0/3	NA	Master
R6	xe-0/0/1	NA	Stateful
	xe-0/0/2	NA	Stateful
	xe-0/0/3	NA	Master

The configuration details on devices R0 through R6 are furnished below.

Example 5.8 Configuration of g.8275.1 profile on R0

```
user@R0# show protocols ptp
clock-mode boundary;
profile-type g.8275.1;
priority2 1;
phy-timestamping;
slave {
    hybrid;
}
master {
    interface ae1.0 {
        multicast-mode {
            transport {
                ieee-802.3 link-local;
            }
        }
        primary xe-0/0/4;
        secondary xe-0/0/5;
    }
}
stateful {
    interface xe-0/0/1.0 {
        multicast-mode {
            transport {
                ieee-802.3 link-local;
            }
        }
    }
    interface ae0.0 {
        multicast-mode {
            transport {
                ieee-802.3 link-local;
            }
        }
        primary xe-0/0/2;
        secondary xe-0/0/3;
    }
}
```

Example 5.9 Configuration of chassis synchronization on R0

```
user@R0# show chassis
network-services enhanced-ip;
synchronization {
    network-option option-1;
    selection-mode received-quality;
    quality-mode-enable;
    source {
        interfaces xe-0/0/1 {
            priority 1;
            wait-to-restore 0;
            quality-level prc;
        }
        interfaces xe-0/0/2 {
            priority 2;
            wait-to-restore 0;
            aggregated-ether ae0;
            quality-level prc;
        }
        interfaces xe-0/0/3 {
            priority 2;
            wait-to-restore 0;
            aggregated-ether ae0;
            quality-level prc;
        }
    }
    esmc-transmit {
        interfaces all;
    }
}
```

This configuration uses `link-local` multicast MAC address (01:80:c2:00:00:0e) for the PTP communications. However, when the user doesn't specify the `link-local` knob under the PTP configuration hierarchy, it means the communication uses a non-link-local MAC address (01:1b:19:00:00:00). For proper working of PTP, both ends of the link should have similar configurations.

Example 5.10 Configuration of g.8275.1 profile on R1

```
user@R1# show protocols ptp
clock-mode boundary;
profile-type g.8275.1;
priority2 2;
phy-timestamping;
slave {
    hybrid;
}
master {
    interface ae1.0 {
        multicast-mode {
            transport {
                ieee-802.3 link-local;
            }
        }
        primary xe-0/0/4;
        secondary xe-0/0/5;
    }
}
stateful {
    interface xe-0/0/1.0 {
        multicast-mode {
            transport {
                ieee-802.3 link-local;
```

```
91                  }
92              }
93          }
94          interface ae0.0 {
95              multicast-mode {
96                  transport {
97                      ieee-802.3 link-local;
98                  }
99              }
100             primary xe-0/0/2;
101             secondary xe-0/0/3;
102         }
103     }
```

Example 5.11 Configuration of chassis synchronization on R1

```
104     user@R1# show chassis
105     network-services enhanced-ip;
106     synchronization {
107         network-option option-1;
108         selection-mode received-quality;
109         quality-mode-enable;
110         source {
111             interfaces xe-0/0/1 {
112                 priority 1;
113                 wait-to-restore 0;
114                 quality-level prc;
115             }
116             interfaces xe-0/0/2 {
117                 priority 2;
118                 wait-to-restore 0;
119                 aggregated-ether ae0;
120                 quality-level prc;
121             }
122             interfaces xe-0/0/3 {
123                 priority 2;
124                 wait-to-restore 0;
125                 aggregated-ether ae0;
126                 quality-level prc;
127             }
128         }
129         esmc-transmit {
130             interfaces all;
131         }
132     }
```

Example 5.12 Configuration of g.8275.1 profile on R2

```
133     user@R2# show protocols ptp
134     clock-mode boundary;
135     profile-type g.8275.1;
136     priority2 3;
137     phy-timestamping;
138     slave {
139         hybrid;
140     }
141     master {
142         interface xe-0/0/5.0 {
143             multicast-mode {
144                 transport {
145                     ieee-802.3 link-local;
146                 }
147             }
148         }
149     }
150     stateful {
151         interface ae0.0 {
152             multicast-mode {
```

```
153                 transport {
154                     ieee-802.3 link-local;
155                 }
156             }
157             primary xe-0/0/1;
158             secondary xe-0/0/2;
159         }
160         interface ae1.0 {
161             multicast-mode {
162                 transport {
163                     ieee-802.3 link-local;
164                 }
165             }
166             primary xe-0/0/3;
167             secondary xe-0/0/4;
168         }
169     }
```

Example 5.13 Configuration of chassis synchronization on R2

```
170     user@R2# show chassis
171     network-services enhanced-ip;
172     synchronization {
173         network-option option-1;
174         selection-mode received-quality;
175         quality-mode-enable;
176         source {
177             interfaces xe-0/0/1 {
178                 priority 1;
179                 wait-to-restore 0;
180                 aggregated-ether ae0;
181                 quality-level prc;
182             }
183             interfaces xe-0/0/2 {
184           priority 1;
185                 wait-to-restore 0;
186                 aggregated-ether ae0;
187                 quality-level prc;
188             }
189             interfaces xe-0/0/3 {
190                 priority 2;
191                 wait-to-restore 0;
192                 aggregated-ether ae1;
193                 quality-level prc;
194             }
195       interfaces xe-0/0/4 {
196                 priority 2;
197                 wait-to-restore 0;
198                 aggregated-ether ae1;
199                 quality-level prc;
200             }
201         }
202         esmc-transmit {
203             interfaces all;
204         }
205     }
```

Example 5.14 Configuration of g.8275.1 profile on R3

```
206     user@R3# show protocols ptp
207     clock-mode boundary;
208     profile-type g.8275.1;
209     priority2 4;
210     phy-timestamping;
211     slave {
212         hybrid;
213     }
214     master {
```

```
215          interface xe-0/0/5.0 {
216              multicast-mode {
217                  transport {
218                      ieee-802.3 link-local;
219                  }
220              }
221          }
222      }
223      stateful {
224          interface ae0.0 {
225              multicast-mode {
226                  transport {
227                      ieee-802.3 link-local;
228                  }
229              }
230              primary xe-0/0/1;
231              secondary xe-0/0/2;
232          }
233          interface ae1.0 {
234              multicast-mode {
235                  transport {
236                      ieee-802.3 link-local;
237                  }
238              }
239              primary xe-0/0/3;
240              secondary xe-0/0/4;
241          }
242      }
```

Example 5.15 Configuration of chassis synchronization on R3

```
243      user@R2# show chassis
244      network-services enhanced-ip;
245      synchronization {
246          network-option option-1;
247          selection-mode received-quality;
248          quality-mode-enable;
249          source {
250              interfaces xe-0/0/1 {
251                  priority 1;
252                  wait-to-restore 0;
253                  aggregated-ether ae0;
254                  quality-level prc;
255             }
256              interfaces xe-0/0/2 {
257                  priority 1;
258                  wait-to-restore 0;
259                  aggregated-ether ae0;
260                  quality-level prc;
261              }
262              interfaces xe-0/0/3 {
263                  priority 2;
264                  wait-to-restore 0;
265                  aggregated-ether ae1;
266                  quality-level prc;
267              }
268        interfaces xe-0/0/4 {
269                  priority 2;
270                  wait-to-restore 0;
271                  aggregated-ether ae1;
272                  quality-level prc;
273              }
274          }
275          esmc-transmit {
276              interfaces all;
277          }
278      }
```

Example 5.16 Configuration of g.8275.1 profile on R4

```
user@R4# show protocols ptp
clock-mode boundary;
profile-type g.8275.1;
priority2 5;
phy-timestamping;
slave {
    hybrid;
}
master {
    interface xe-0/0/3.0 {
        multicast-mode {
            transport {
                ieee-802.3 link-local;
            }
        }
    }
}
stateful {
    interface xe-0/0/1.0 {
        multicast-mode {
            transport {
                ieee-802.3 link-local;
            }
        }
    }
    interface xe-0/0/2.0 {
        multicast-mode {
            transport {
                ieee-802.3 link-local;
            }
        }
    }
}
```

Example 5.17 Configuration of chassis synchronization on R4

```
user@R4# show chassis
network-services enhanced-ip;
synchronization {
    network-option option-1;
    selection-mode received-quality;
    quality-mode-enable;
    source {
        interfaces xe-0/0/1 {
            priority 1;
            wait-to-restore 0;
            quality-level prc;
        }
        interfaces xe-0/0/2 {
            priority 2;
            wait-to-restore 0;
            quality-level prc;
        }
    }
    esmc-transmit {
        interfaces all;
    }
}
```

Example 5.18 Configuration of g.8275.1 profile on R5

```
user@R5# show protocols ptp
clock-mode boundary;
profile-type g.8275.1;
priority2 6;
```

```
338      phy-timestamping;
339      slave {
340          hybrid;
341      }
342      master {
343          interface xe-0/0/3.0 {
344              multicast-mode {
345                  transport {
346                      ieee-802.3 link-local;
347                  }
348              }
349          }
350      }
351      stateful {
352          interface xe-0/0/1.0 {
353              multicast-mode {
354                  transport {
355                      ieee-802.3 link-local;
356                  }
357              }
358          }
359          interface xe-0/0/2.0 {
360              multicast-mode {
361                  transport {
362                      ieee-802.3 link-local;
363                  }
364              }
365          }
366      }
```

Example 5.19 Configuration of chassis synchronization on R5

```
367      user@R5# show chassis
368      network-services enhanced-ip;
369      synchronization {
370          network-option option-1;
371          selection-mode received-quality;
372          quality-mode-enable;
373          source {
374              interfaces xe-0/0/1 {
375                  priority 1;
376                  wait-to-restore 0;
377                  quality-level prc;
378              }
379              interfaces xe-0/0/2 {
380                  priority 2;
381                  wait-to-restore 0;
382                  quality-level prc;
383              }
384          }
385          esmc-transmit {
386              interfaces all;
387          }
388      }
```

Example 5.20 Configuration of g.8275.1 profile on R6

```
389      user@R6# show protocols ptp
390      clock-mode boundary;
391      profile-type g.8275.1;
392      priority2 1;
393      stateful {
394          interface xe-0/0/1.0 {
395              multicast-mode {
396                  slave-candidate;
397                  transport {
398                      ieee-802.3 link-local;
399                  }
```

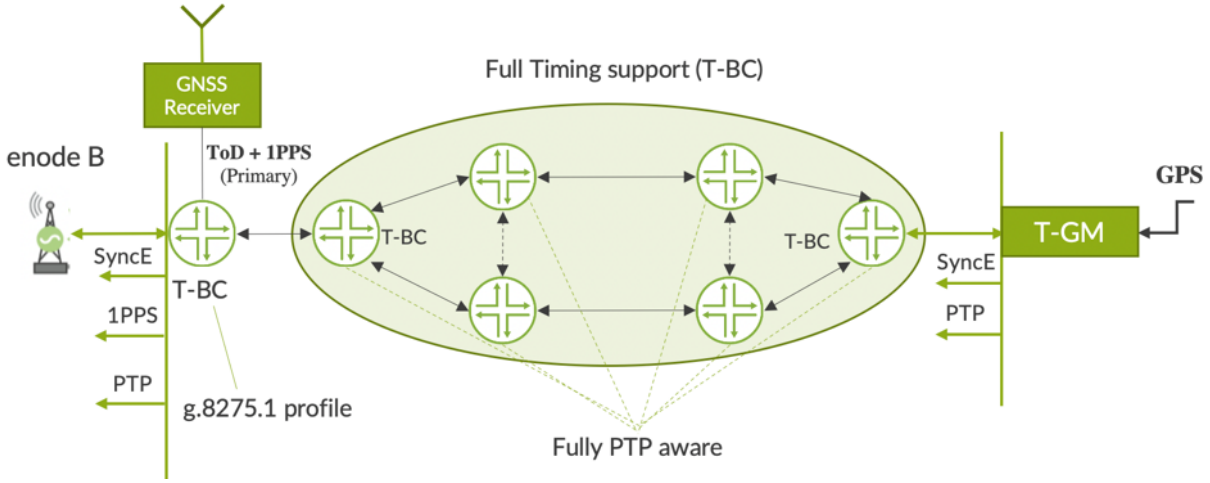
```
400             }
401         }
402         interface xe-0/0/2.0 {
403             multicast-mode {
 404                slave-candidate;
405                 transport {
406                     ieee-802.3 link-local;
407                 }
408             }
409         }
410     }
```

Example 5.21 Configuration of chassis synchronization on R6

```
411     user@R5# show chassis
412     network-services enhanced-ip;
413     synchronization {
414         network-option option-1;
415         selection-mode received-quality;
416         quality-mode-enable;
417         source {
418             interfaces xe-0/0/1 {
419                 priority 1;
420                 wait-to-restore 0;
421                 quality-level prc;
422             }
423             interfaces xe-0/0/2 {
424                 priority 2;
425                 wait-to-restore 0;
426                 quality-level prc;
427             }
428         }
429         esmc-transmit {
430             interfaces all;
431         }
432     }
```

You can also use the g.8275.1 network as a backup to GNSS-assisted T-BC as depicted in Figure 5.5. This requires virtual-port support on the T-BC to recover the time via the external timing inputs ToD and 1PPS.

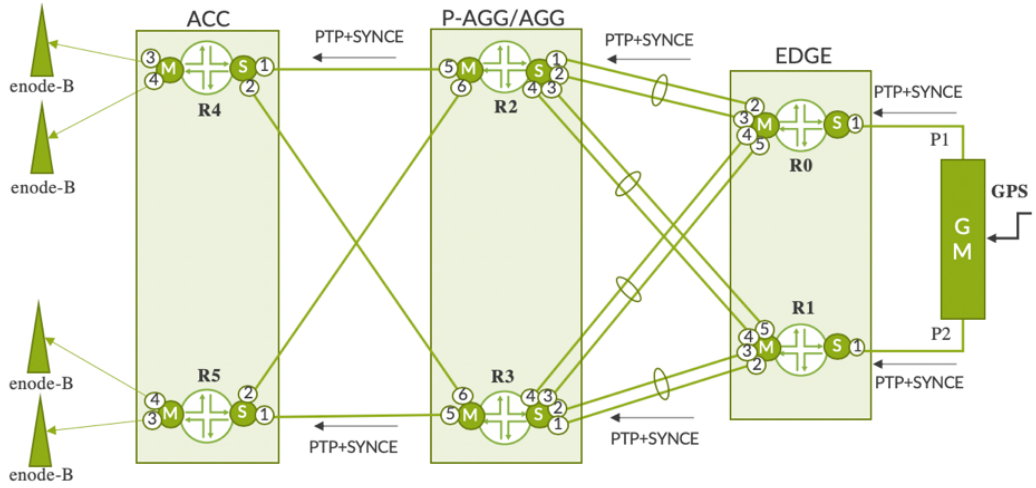
Figure 5.5 End-to-End Hybrid with GNSS Assisted Solution



End-to-End G.8275.1.ENH Profile with Full On-path Support

In this deployment scenario, PTP is enabled over IPv4 transport using the G.8275.1.enh profile. The link between R0 and (R2, R3) and R1 and (R2, R3) are Aggregated Ethernet (AE) as shown in Figure 5.6. The configured port roles are summarized in Table 5.4.

Figure 5.6 End-to-End Hybrid with the G.8275.1.enh Profile



In the case of PTP over AE, you should designate one IFL as primary and another IFL as secondary under the PTP stanza. In hybrid mode of PTP over LAG, the primary and secondary interfaces must reside on the same line card. Usually for PTP master or PTP client, streams are created on the FPC on which the primary IFL is residing. Announce and sync packets are transmitted on this primary PTP AE link'. Delay request packets would also be received on the same link, as that same link would be configured as primary at the remote end, too. The line card containing this active PTP AE link would receive announce/sync packets from the remote master.

Table 5.4 Ports Operating Mode

Nodes	Port	Member	Port Role
R0	xe-0/0/1	NA	Client
	ae0	xe-0/0/2(Primary) xe-0/0/3(Secondary)	Master
	ae1	xe-0/0/4(Primary) xe-0/0/5(Secondary)	Master
R1	xe-0/0/1	NA	Client
	ae0	xe-0/0/2(Primary) xe-0/0/3(Secondary)	Master
	ae1	xe-0/0/4(Primary) xe-0/0/5(Secondary)	Master
R2	ae0	xe-0/0/1(Primary) xe-0/0/2(Secondary)	Client
	ae1	xe-0/0/4(Primary) xe-0/0/3(Secondary)	Client
	xe-0/0/5	NA	Master
	xe-0/0/6	NA	Master
R3	ae0	xe-0/0/1(Primary) xe-0/0/2(Secondary)	Client
	ae1	xe-0/0/4(Primary) xe-0/0/3(Secondary)	Client
	xe-0/0/5	NA	Master
	xe-0/0/6	NA	Master
R4	xe-0/0/1	NA	Client
	xe-0/0/2	NA	Client
	xe-0/0/3	NA	Master
	xe-0/0/4	NA	Master
R5	xe-0/0/1	NA	Client
	xe-0/0/2	NA	Client
	xe-0/0/3	NA	Master
	xe-0/0/4	NA	Master

The configuration details on devices R0 through R6 are furnished here.

Example 5.22 Configuration of g.8275.1.enh profile on R0

```
user@R0# show protocols ptp
clock-mode boundary;
profile-type g.8275.1.enh;
priority2 2;
phy-timestamping;
slave {
    interface xe-0/0/1.0 {
        unicast-mode {
            transport ipv4;
            clock-source 10.0.0.1 local-ip-address 10.0.0.2;
        }
    }
    hybrid;
}
master {
    interface ae0.0 {
        unicast-mode {
            transport ipv4;
            clock-client 11.0.0.2/32 local-ip-address 11.0.0.1;
        }
  primary xe-0/0/2;
  secondary xe-0/0/3;
    }
    interface ae1.0 {
        unicast-mode {
            transport ipv4;
            clock-client 12.0.0.2/32 local-ip-address 12.0.0.1;
        }
        primary xe-0/0/4;
        secondary xe-0/0/5;
    }
}
```

Example 5.23 Configuration of chassis synchronization on R0

```
user@R0# show chassis
network-services enhanced-ip;
synchronization {
    network-option option-1;
    selection-mode received-quality;
    quality-mode-enable;
    source {
        interfaces xe-0/0/1 {
            wait-to-restore 0;
            quality-level prc;
        }
    }
    esmc-transmit {
        interfaces all;
    }
}
```

Example 5.24 Configuration of g.8275.1.enh profile on R1

```
user@R1# show protocols ptp
clock-mode boundary;
profile-type g.8275.1.enh;
priority2 2;
phy-timestamping;
slave {
    interface xe-0/0/1.0 {
        unicast-mode {
            transport ipv4;
```

```
58                  clock-source 20.0.0.1 local-ip-address 20.0.0.2;
59              }
60          }
61          hybrid;
62      }
63      master {
64          interface ae0.0 {
65              unicast-mode {
66                  transport ipv4;
67                  clock-client 21.0.0.2/32 local-ip-address 21.0.0.1;
68              }
69        primary xe-0/0/2;
70        secondary xe-0/0/3;
71          }
72          interface ae1.0 {
73              unicast-mode {
74                  transport ipv4;
75                  clock-client 22.0.0.2/32 local-ip-address 22.0.0.1;
76              }
77              primary xe-0/0/4;
78              secondary xe-0/0/5;
79          }
80      }
```

Example 5.25 Configuration of chassis synchronization on R1

```
81      user@R1# show chassis
82      network-services enhanced-ip;
83      synchronization {
84          network-option option-1;
85          selection-mode received-quality;
86          quality-mode-enable;
87          source {
88              interfaces xe-0/0/1 {
89                  wait-to-restore 0;
90                  quality-level prc;
91              }
92          }
93          esmc-transmit {
94              interfaces all;
95          }
96      }
```

Example 5.26 Configuration of g.8275.1.enh profile on R2

```
97      user@R2# show protocols ptp
98      clock-mode boundary;
99      profile-type g.8275.1.enh;
100     priority2 2;
101     phy-timestamping;
102     slave {
103         interface ae0.0 {
104             unicast-mode {
105                 transport ipv4;
106                 clock-source 100.0.0.1 local-ip-address 100.0.0.2;
107             }
108       primary xe-0/0/1;
109           secondary xe-0/0/2;
110         }
111         interface ae1.0 {
112             unicast-mode {
113                 transport ipv4;
114                 clock-source 100.0.0.1 local-ip-address 100.0.0.2;
115             }
116       primary xe-0/0/3;
117           secondary xe-0/0/4;
118         }
119         hybrid;
```

```
120      }
121      master {
122          interface xe-0/0/5.0 {
123              unicast-mode {
124                  transport ipv4;
125                  clock-client 12.0.0.2/32 local-ip-address 12.0.0.1;
126              }
127          }
128          interface xe-0/0/6.0 {
129              unicast-mode {
130                  transport ipv4;
131                  clock-client 11.0.0.2/32 local-ip-address 11.0.0.1;
132              }
133          }
134      }
```

Example 5.27 Configuration of chassis synchronization on R1

```
135      user@R2# show chassis
136      network-services enhanced-ip;
137      synchronization {
138          network-option option-1;
139          selection-mode received-quality;
140          quality-mode-enable;
141          source {
142              interfaces xe-0/0/1 {
143                  priority 3;
144                  wait-to-restore 0;
145                  aggregated-ether ae0;
146                  quality-level prc;
147              }
148              interfaces xe-0/0/2 {
149                  priority 2;
150                  wait-to-restore 0;
151                  aggregated-ether ae0;
152                  quality-level prc;
153              }
154              interfaces xe-0/0/3 {
155                  priority 2;
156                  wait-to-restore 0;
157                  aggregated-ether ae1;
158                  quality-level prc;
159              }
160              interfaces xe-0/0/4 {
161                  priority 3;
162                  wait-to-restore 0;
163                  aggregated-ether ae1;
164                  quality-level prc;
165              }
166          }
167          esmc-transmit {
168              interfaces all;
169          }
170      }
```

Example 5.28 Configuration of g.8275.1.enh profile on R3

```
171      user@R3# show protocols ptp
172      clock-mode boundary;
173      profile-type g.8275.1.enh;
174      priority2 2;
175      phy-timestamping;
176      slave {
177          interface ae0.0 {
178              unicast-mode {
179                  transport ipv4;
180                  clock-source 100.0.0.1 local-ip-address 100.0.0.2;
181              }
```

```
182         primary xe-0/0/1;
183               secondary xe-0/0/2;
184           }
185           interface ae1.0 {
186               unicast-mode {
187                   transport ipv4;
188                   clock-source 100.0.0.1 local-ip-address 100.0.0.2;
189               }
190         primary xe-0/0/3;
191         secondary xe-0/0/4;
192           }
193           hybrid;
194       }
195       master {
196           interface xe-0/0/5.0 {
197               unicast-mode {
198                   transport ipv4;
199                   clock-client 12.0.0.2/32 local-ip-address 12.0.0.1;
200               }
201           }
202           interface xe-0/0/6.0 {
203               unicast-mode {
204                   transport ipv4;
205                   clock-client 11.0.0.2/32 local-ip-address 11.0.0.1;
206               }
207           }
208       }
```

Example 5.29 Configuration of chassis synchronization on R3

```
209       user@R3# show chassis
210       network-services enhanced-ip;
211       synchronization {
212           network-option option-1;
213           selection-mode received-quality;
214           quality-mode-enable;
215           source {
216               interfaces xe-0/0/1 {
217                   priority 3;
218                   wait-to-restore 0;
219                   aggregated-ether ae0;
220                   quality-level prc;
221               }
222               interfaces xe-0/0/2 {
223                   priority 2;
224                   wait-to-restore 0;
225                   aggregated-ether ae0;
226                   quality-level prc;
227               }
228               interfaces xe-0/0/3 {
229                   priority 2;
230                   wait-to-restore 0;
231                   aggregated-ether ae1;
232                   quality-level prc;
233               }
234               interfaces xe-0/0/4 {
235                   priority 3;
236                   wait-to-restore 0;
237                   aggregated-ether ae1;
238                   quality-level prc;
239               }
240           }
241           esmc-transmit {
242               interfaces all;
243           }
244       }
```

End-to-End G.8275.2 Profile with Partial or Assisted Partial On-path Support

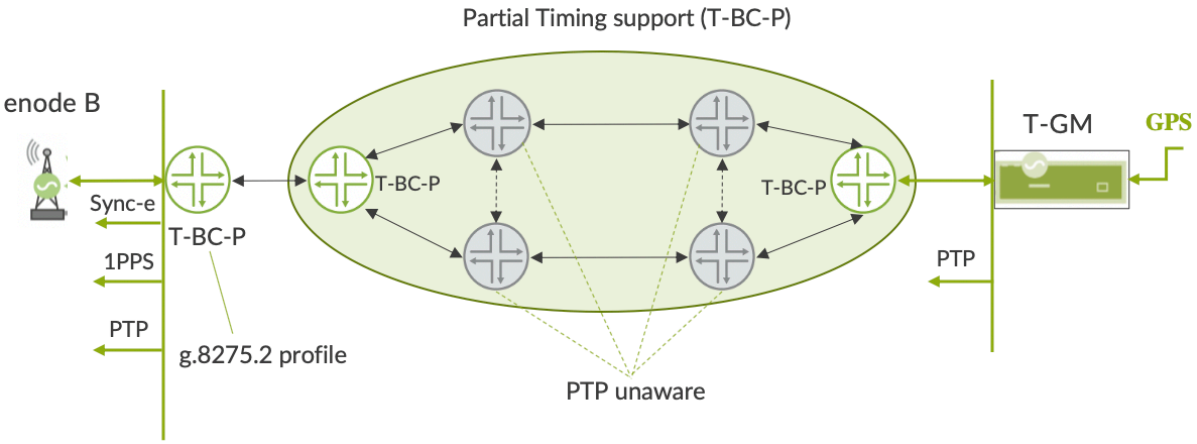
A partial timing support network consists of a mix of both PTP aware and unaware devices. Typically, Telecom-boundary clocks (T-BC) or Telecom-Time client clocks (T-TSC) are used in the partial timing support employing the ITU-T G.8275.2 profile. Let's list a few of the possibilities:

- Partial timing network with G.8275.2/G.8275.2.enh profile
- Assisted partial timing network with G.8275.2/G.8275.2.enh profile
- Full timing support network followed by an assisted partial timing support network
- Full timing support network followed by a partial timing support network
- Assisted partial timing support network followed by a full timing support network
- Partial timing support network followed by a full timing support network

Partial Timing Network With G.8275.2.Enh Profile

In Figure 5.7, T-GM uses the G.8275.2 profile and delivers PTP clock to T-BC-P. The network consists of PTP-aware and PTP-unaware devices. PTP-unaware devices route the PTP packets just like any other IP packet, to the destination T-BC-P. You need to apply the right QoS treatment to PTP packets while they are forwarded by the PTP-unaware devices in between. Refer to the *Examples 3.35* through *3.38*, in Chapter 3, for configuration details with the g.8275.2.enh profile.

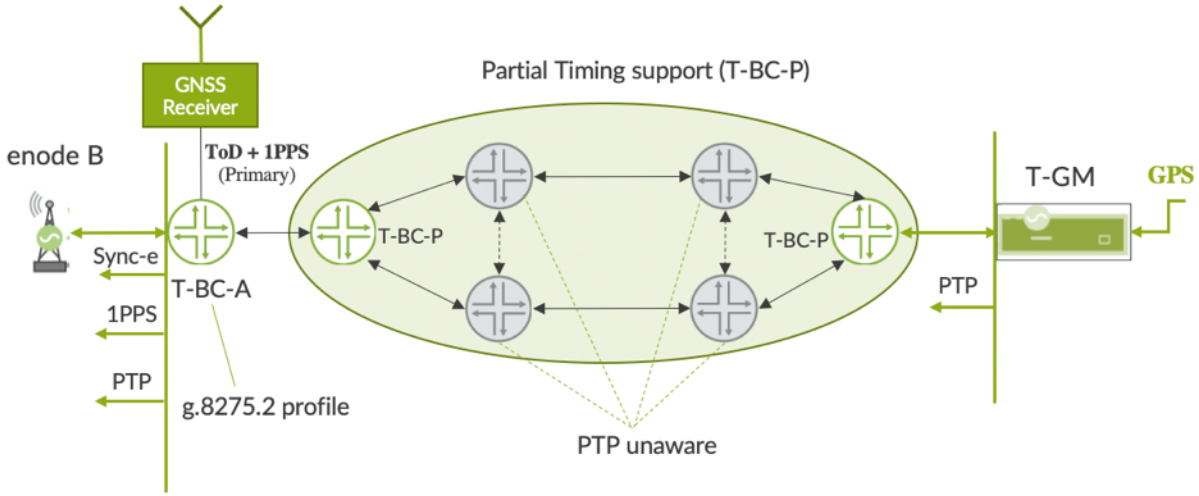
Figure 5.7 Partial Timing Network with the G.8275.2.enh Profile



Assisted Partial Timing Network With G.8275.2.Enh Profile

In this deployment, T-BC-A selects (ToD + 1PPS) as primary clock source and delivers phase to the base station (see Figure 5.8). T-BC-A could use multi-profile so that it could use G.8275.1 profile towards enode B. If (ToD + 1PPS) are not available for any reason, the clock from the backup partial timing network path is selected by T-BC-A. Again, refer to the *Examples 3.35 through 3.38* in Chapter 3 for configuration details with g.8275.2.enh profile.

Figure 5.8 Assisted Partial Timing Network with the G.8275.2.enh Profile

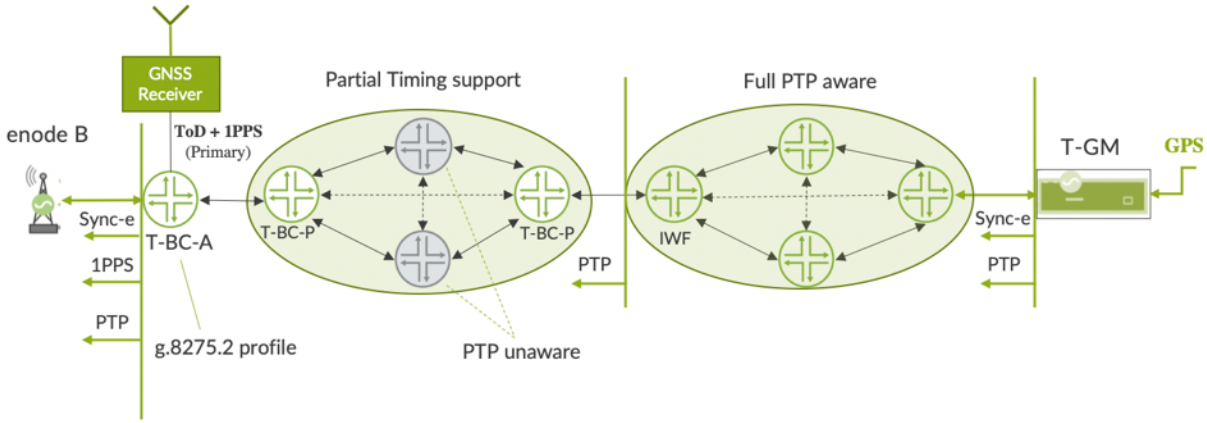


Full Timing Support Network Followed By An Assisted Partial Timing Support Network

In this deployment in Figure 5.9, IWF enables the multi-profile support on a given node: the g.8275.1 profile for interwork with Full PTP aware network and the g.8275.2 profile for interwork with partial timing network. Refer to the *Examples 3.35* through *3.38* for the g.8275.2.enh profile configurations, and *Examples 3.19* to *3.20* for the g.8275.1 profile configurations in Chapter 3.

NOTE At the time of writing this book, Juniper devices don't support multi-profile. This support may come in a future release.

Figure 5.9 Full Timing Support Followed by Assisted Partial Timing Network

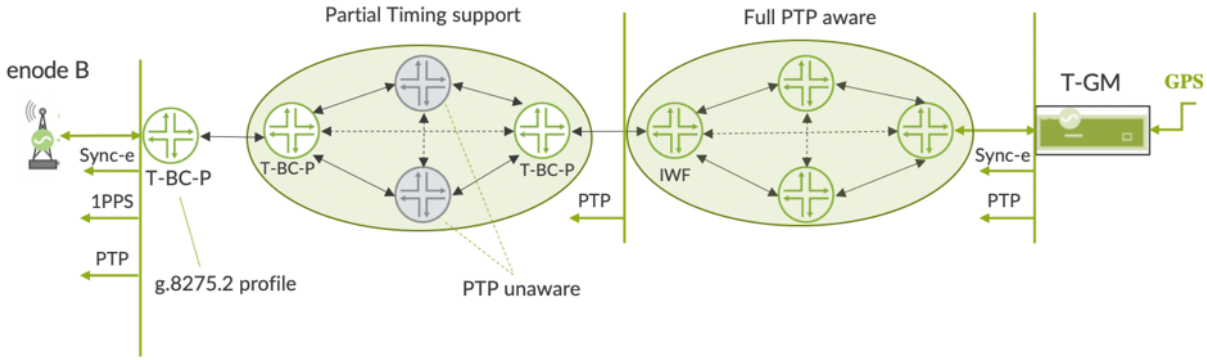


Full Timing Support Network Followed By An Partial Timing Support Network

In Figure 5.10, IWF enables the multi-profile support on a given node, the g.8275.1 profile for interwork with full PTP aware network and the g.8275.2 profile for interwork with the partial timing network. Refer to Chapter 3, *Examples 3.35 - 3.38* for the g.8275.2.enh profile configurations and *Examples 3.19 - 3.20* for the g.8275.1 profile configs.

NOTE At the time of writing this book, Juniper devices don't support multi-profile. This support may come in a future release.

Figure 5.10 Full Timing Support Followed by Partial Timing Network



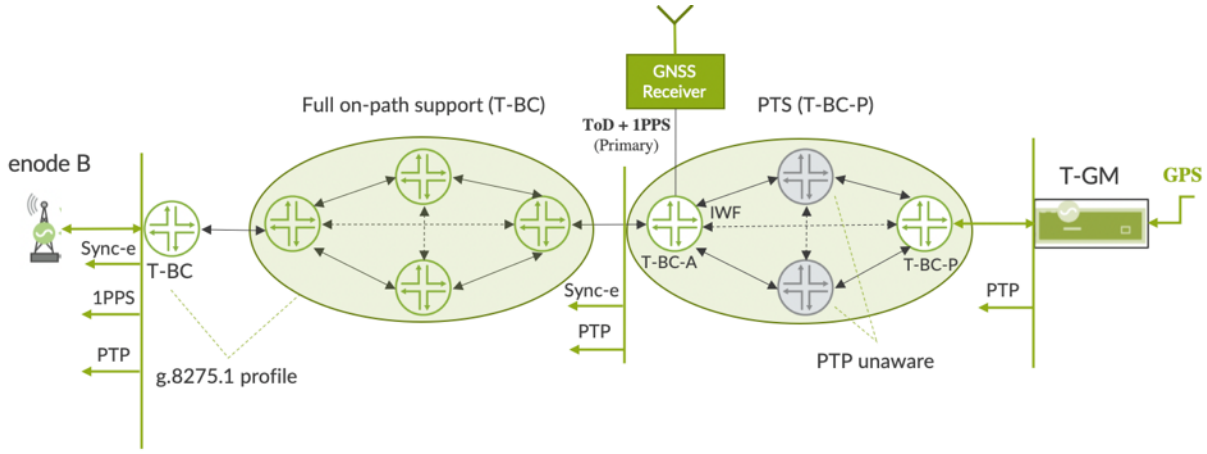
Assisted Partial Timing Support Network Followed By Full Timing Support Network

In this deployment IWF enables the multi-profile support on T-BC-A, the g.8275.1 profile to interwork with the full PTP aware network in the downstream and the g.8275.2 profile to interwork with the partial timing network in the upstream. T-BC-A selects (ToD + 1PPS) as the primary clock source via virtual-port and delivers PTP and SyncE to the downstream network. Virtual port could be part of either the g.8275.1 profile or g.8275.2 profile. You can refer to the *Examples 3.35* through

3.38 for the g.8275.2.enh profile configurations and *Examples 3.19* to *3.20* for the g.8275.1 profile configurations.

NOTE At the time of writing this book, Juniper devices don't support multi-profile. This support may come in a future release.

Figure 5.11 Assisted Partial Network Followed by Full Timing Network

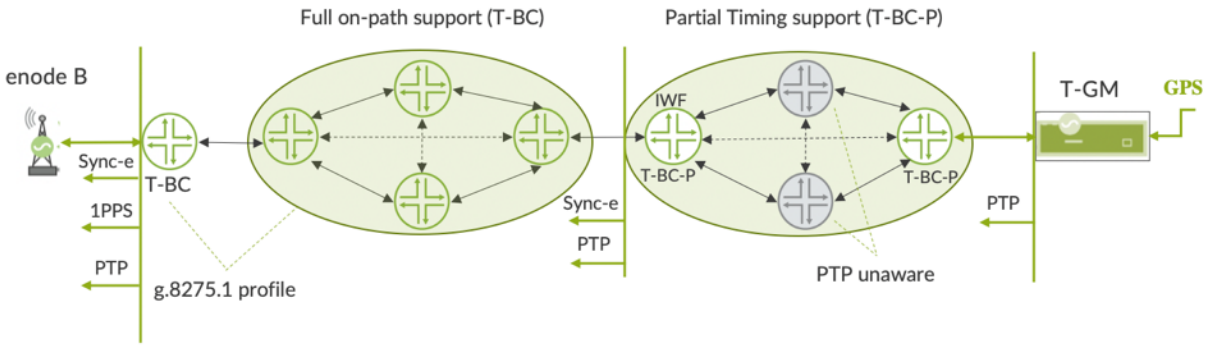


Partial Timing Support Network Followed By Full Timing Support Network

In the final sample deployment (see Figure 5.12), IWF enables the multi-profile support on T-BC-A, g.8275.1 profile for interwork with full PTP aware network in the downstream and then g.8275.2 profile for interwork with partial timing network in the upstream. You can refer the *Examples 3.35* through *3.38* for the g.8275.2.enh profile configurations and *Examples 3.19* to *3.20* for the g.8275.1 profile configurations.

NOTE At the time of writing this book, Juniper devices don't support multi-profile. This support may come in a future release.

Figure 5.12 Partial Network Followed by Full Timing Network

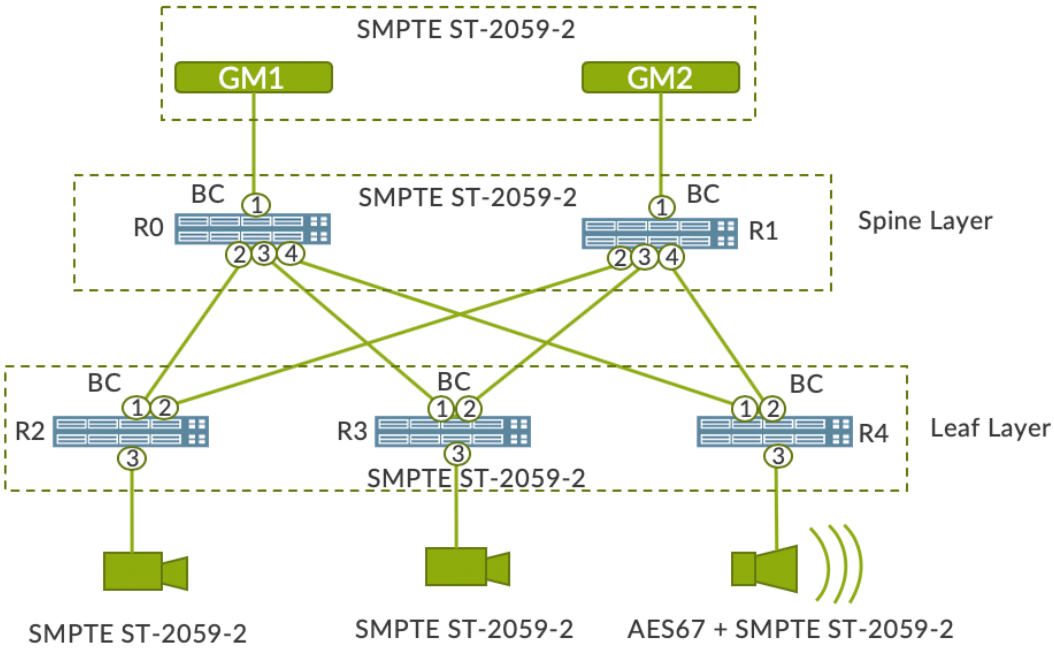


Media-Profile Deployment with SMPTE/AES67 Profile

The broadcast industry is undergoing a massive and rapid IP transformation as it moves from the existing Serial Digital Interface (SDI) infrastructure to an IP infrastructure to enable higher resolution video, better infrastructure connectivity in live production, and various other star-studded use cases. Here the endpoints such as cameras, video switchers, and audio devices are to be time synchronized with respect to a common time reference. The IP infrastructure enables PTP to distribute time-to-end devices.

Figure 5.13 is one such spine-leaf deployment with a broadcast use case. Here, the leaf layer consists of the access switches that connect to the endpoints such as a camera or a video switcher or audio devices. PTP-GM is connected to the spine and distributes the time to the endpoints via the leaf devices.

Figure 5.13 PTP Media-profile-Spine-Leaf Architecture



The configuration details on devices R0 through R4 are furnished below.

Example 5.30 Configuration of media profile on R0

```
user@R0# show protocols ptp
clock-mode boundary;
profile-type smpte;
slave {
    interface xe-0/0/1.0 {


        multicast-mode {
            transport {
                ipv4;
```

```
                    }
                    local-ip-address 10.0.0.1;
                }
            }
        }
        master {
            interface xe-0/0/2.0 {
                multicast-mode {
                    transport {
                        ipv4;
                    }
                    local-ip-address 20.0.0.1;
                }
            }
            interface xe-0/0/3.0 {
                multicast-mode {
                    transport {
                        ipv4;
                    }
                    local-ip-address 30.0.0.1;
                }
            }
            interface xe-0/0/4.0 {
                multicast-mode {
                    transport {
                        ipv4;
                    }
                    local-ip-address 40.0.0.1;
                }
            }
        }
```

Example 5.31 Configuration of media profile on R1

```
        user@R1# show protocols ptp
        clock-mode boundary;
        profile-type smpte;
        slave {
            interface xe-0/0/1.0 {
                multicast-mode {
                    transport {
                        ipv4;
                    }
                    local-ip-address 10.0.1.1;
                }
            }
        }
        master {
            interface xe-0/0/2.0 {
                multicast-mode {
                    transport {
                        ipv4;
                    }
                    local-ip-address 20.0.1.1;
                }
            }
            interface xe-0/0/3.0 {
                multicast-mode {
                    transport {
```

```
                    ipv4;
                }
                local-ip-address 30.0.1.1;
            }
        }
        interface xe-0/0/4.0 {
            multicast-mode {
                transport {
                    ipv4;
                }
                local-ip-address 40.0.1.1;
            }
        }
    }
```

Example 5.32 Configuration of media profile on R2

```
user@R2# show protocols ptp
clock-mode boundary;
profile-type smpte;
slave {
    interface xe-0/0/1.0 {
        multicast-mode {
            transport {
                ipv4;
            }
            local-ip-address 20.0.0.2;
        }
    }
    interface xe-0/0/2.0 {
        multicast-mode {
            transport {
                ipv4;
            }
            local-ip-address 20.0.1.2;
        }
    }
}
master {
    interface xe-0/0/3.0 {
        multicast-mode {
            transport {
                ipv4;
            }
            local-ip-address 20.0.2.1;
        }
    }
}
```

Example 5.33 Configuration of media profile on R3

```
user@R3# show protocols ptp
clock-mode boundary;
profile-type smpte;
slave {
    interface xe-0/0/1.0 {
        multicast-mode {
            transport {
                ipv4;
            }
            local-ip-address 30.0.0.2;
        }
    }
```

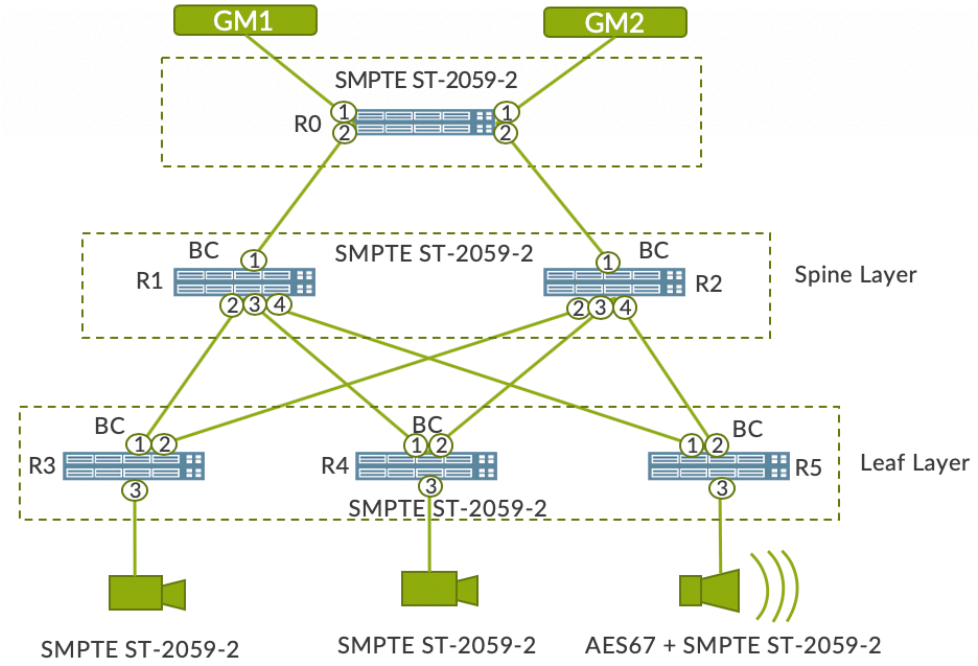
```
122          interface xe-0/0/2.0 {
123              multicast-mode {
124                  transport {
125                      ipv4;
126                  }
127                  local-ip-address 30.0.1.2;
128              }
129          }
130      }
131      master {
132          interface xe-0/0/3.0 {
133              multicast-mode {
134                  transport {
135                      ipv4;
136                  }
137                  local-ip-address 30.0.2.1;
138              }
139          }
140      }
```

Example 5.34 Configuration of media profile on R4

```
141      user@R4# show protocols ptp
142      clock-mode boundary;
143      profile-type smpte;
144      slave {
145          interface xe-0/0/1.0 {
146              multicast-mode {
147                  transport {
148                      ipv4;
149                  }
150                  local-ip-address 40.0.0.2;
151              }
152          }
153          interface xe-0/0/2.0 {
154              multicast-mode {
155                  transport {
156                      ipv4;
157                  }
158                  local-ip-address 40.0.1.2;
159              }
160          }
161      }
162      master {
163          interface xe-0/0/3.0 {
164              multicast-mode {
165                  transport {
166                      ipv4;
167                  }
168                  local-ip-address 40.0.2.1;
169              }
170          }
171      }
```

With redundant network deployments, an external PTP feeder switch can be used as a boundary clock with media profile enabled as shown in Figure 5.14 below.

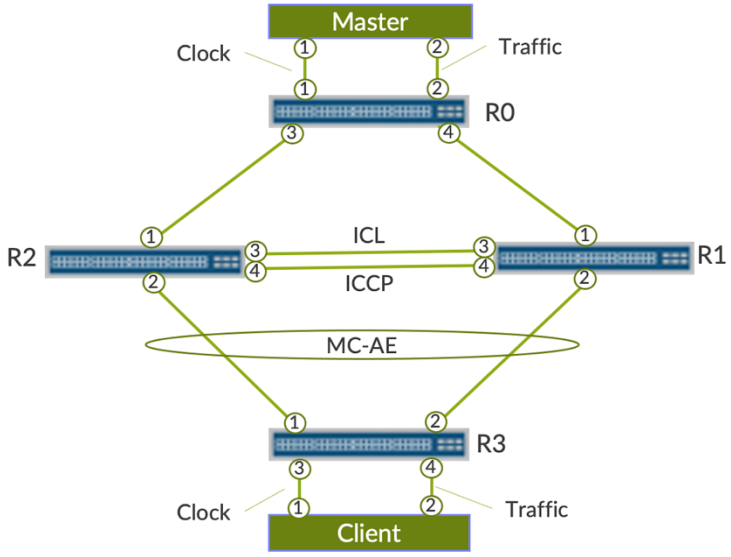
Figure 5.14 PTP Media-profile-Spine-Leaf Architecture-PTP Feeder



TCv6 Deployment with MC-LAG & IRB

In Figure 5.15, TC is configured on all the devices. The tester connected to R0 and R3 is configured as the PTP master and client, respectively. MC-AE is configured between R1 and R2. Data traffic is also sent between R0 and R3 to verify the TC performance in presence of the data traffic. Complete configurations are furnished in Examples 5.35 to 5.52.

Figure 5.15 TCv6 with MC-LAG and IRB



Example 5.35 Interface configuration on R1

```
user@R1# show interfaces
xe-0/0/2 {
    gigether-options {
        802.3ad ae0;
    }
}
xe-0/0/1 {
    unit 0 {
        family inet {
            address 40.0.0.2/24;
        }
        family inet6 {
            address 4010::9/64;
        }
    }
}
xe-0/0/3 {
    gigether-options {
        802.3ad ae1;
    }
}
xe-0/0/4 {
    unit 0 {
        family inet6 {
            address 2000::1/64;
        }
    }
}
ae0 {
    flexible-vlan-tagging;
    encapsulation flexible-ethernet-services;
    aggregated-ether-options {
        lacp {
            active;
            periodic fast;
            system-priority 100;
            system-id 10:10:10:10:10:10;
            admin-key 1;
        }
        mc-ae {
            mc-ae-id 1;
            redundancy-group 1;
            chassis-id 0;
            mode active-active;
            status-control active;
        }
    }
    unit 0 {
        encapsulation vlan-bridge;
        vlan-id 1001;
        multi-chassis-protection 2.2.2.2 {
            interface ae1.2;
        }
    }
}
ae1 {
    flexible-vlan-tagging;
    encapsulation flexible-ethernet-services;
    aggregated-ether-options {
        link-speed 1g;
        lacp {
            active;
            periodic fast;
            accept-data;
        }
    }
    unit 0 {
```

```
68                vlan-id 101;
69                family inet {
70                    address 11.11.11.1/30;
71                }
72            }
73            unit 2 {
74                encapsulation vlan-bridge;
75                vlan-id 1001;
76            }
77        }
78        irb {
79            gratuitous-arp-reply;
80            arp-l2-validate;
81            unit 0 {
82                family inet {
83                    address 30.0.0.2/24 {
84                        vrrp-group 2 {
85                            virtual-address 30.0.0.101;
86                            accept-data;
87                        }
88                    }
89                }
90                family inet6 {
91                    address 3010::2/64 {
92                        vrrp-inet6-group 1 {
93                            virtual-inet6-address 3010::101;
94                            accept-data;
95                        }
96                    }
97                }
98            }
99        }
100       lo0 {
101           unit 0 {
102               family inet {
103                   address 1.1.1.1/32 {
104                       primary;
105                   }
106               }
107               family inet6 {
108                   address 2001:db8::1/128 {
109                       primary;
110                   }
111               }
112           }
113       }
```

Example 5.36 Protocol configuration on R1

```
114       user@R1# show protocols
115       iccp {
116           local-ip-addr 1.1.1.1;
117           peer 2.2.2.2 {
118               redundancy-group-id-list 1;
119               liveness-detection {
120                   minimum-interval 1000;
121               }
122           }
123       }
124       ptp {
125           e2e-transparent;
126       }
127       clock-synchronization {
128           traceoptions {
129               file TCv6 size 10m;
130               flag all;
131           }
132       }
133       ospf {
```

```
134          area 0.0.0.0 {
135              interface irb.0;
136              interface lo0.0;
137              interface xe-0/0/1.0;
138              interface em0.0 {
139                  disable;
140              }
141          }
142      }
143      ospf3 {
144          area 0.0.0.0 {
145              interface irb.0;
146              interface lo0.0;
147              interface xe-0/0/1.0;
148              interface em0.0 {
149                  disable;
150              }
151          }
152      }
153      l2-learning {
154          traceoptions {
155              file l2ald size 1g;
156              flag irb;
157              flag all;
158          }
159          mclag-arpreq-sync;
160      }
```

Example 5.37 Chassis configuration on R1

```
161      user@R1# show chassis
162      aggregated-devices {
163          ethernet {
164              device-count 10;
165          }
166      }
```

Example 5.38 Configuration of routing-option on R1

```
167      user@R1# show routing-options
168      static {
169          route 2.2.2.2/32 next-hop 11.11.11.2;
170      }
171      router-id 1.1.1.1;
```

Example 5.39 Configuration of switch-option on R1

```
172      user@R1# show switch-options
173      service-id 10;
```

Example 5.40 Interface configuration on R2

```
174      user@R2# show interfaces
175      xe-0/0/2 {
176          gigether-options {
177              802.3ad ae0;
178          }
179      }
180      xe-0/0/1 {
181          unit 0 {
182              family inet {
183                  address 50.0.0.2/24;
184              }
185              family inet6 {
186                  address 5010::9/64;
187              }
```

```
188         }
189     }
190     xe-0/0/3 {
191         gigether-options {
192             802.3ad ae1;
193         }
194     }
195     xe-0/0/4 {
196         unit 0 {
197             family inet6 {
198                 address 1000::1/64;
199             }
200         }
201     }
202     ae0 {
203         flexible-vlan-tagging;
204         encapsulation flexible-ethernet-services;
205         aggregated-ether-options {
206             lacp {
207                 active;
208                 periodic fast;
209                 system-priority 100;
210                 system-id 10:10:10:10:10:10;
211                 admin-key 1;
212             }
213             mc-ae {
214                 mc-ae-id 1;
215                 redundancy-group 1;
216                 chassis-id 1;
217                 mode active-active;
218                 status-control standby;
219             }
220         }
221         unit 0 {
222             encapsulation vlan-bridge;
223             vlan-id 1001;
224             multi-chassis-protection 1.1.1.1 {
225                 interface ae1.2;
226             }
227         }
228     }
229     ae1 {
230         flexible-vlan-tagging;
231         encapsulation flexible-ethernet-services;
232         aggregated-ether-options {
233             link-speed 1g;
234             lacp {
235                 active;
236                 periodic fast;
237                 accept-data;
238             }
239         }
240         unit 0 {
241             vlan-id 101;
242             family inet {
243                 address 11.11.11.2/30;
244             }
245         }
246         unit 2 {
247             encapsulation vlan-bridge;
248             vlan-id 1001;
249         }
250     }
251     irb {
252         gratuitous-arp-reply;
253         arp-l2-validate;
254         unit 0 {
255             family inet {
256                 address 30.0.0.1/24 {
257                     vrrp-group 2 {
```

```
                        virtual-address 30.0.0.101;
                        accept-data;
                    }
                }
            }
            family inet6 {
                address 3010::1/64 {
                    vrrp-inet6-group 1 {
                        virtual-inet6-address 3010::101;
                        accept-data;
                    }
                }
            }
        }
    }
    lo0 {
        unit 0 {
            family inet {
                address 2.2.2.2/32 {
                    primary;
                }
            }
            family inet6 {
                address 3001:db8::1/128 {
                    primary;
                }
            }
        }
    }
```

Example 5.41 Protocol configuration on R2

```
    user@R2# show protocols
    iccp {
        local-ip-addr 2.2.2.2;
        peer 1.1.1.1 {
            redundancy-group-id-list 1;
            liveness-detection {
                minimum-interval 1000;
            }
        }
    }
    ptp {
        e2e-transparent;
    }
    clock-synchronization {
        traceoptions {
            file TCv6 size 10m;
            flag all;
        }
    }
    ospf {
        area 0.0.0.0 {
            interface irb.0;
            interface lo0.0;
            interface xe-0/0/1.0;
            interface em0.0 {
                disable;
            }
        }
    }
    ospf3 {
        area 0.0.0.0 {
            interface irb.0;
            interface lo0.0;
            interface xe-0/0/1.0;
            interface em0.0 {
```

```
322                 disable;
323             }
324         }
325     }
326     l2-learning {
327         mclag-arpreq-sync;
328       }
```

Example 5.42 Chassis configuration on R2

```
329     user@R2# show chassis
330     aggregated-devices {
331         ethernet {
332             device-count 10;
333         }
334     }
```

Example 5.43 Configuration of routing-option on R2

```
335     user@R2# show routing-options
336     static {
337         route 1.1.1.1/32 next-hop 11.11.11.1;
338     }
```

Example 5.44 Configuration of switch-option on R2

```
339     user@R2# show switch-options
340     service-id 10;
```

Example 5.45 Interface configuration on R3

```
341     user@R3# show interfaces
342     xe-0/0/4 {
343         unit 0 {
344             family inet6 {
345                 address 3080::10/64;
346             }
347         }
348     }
349     xe-0/0/3 {
350         unit 0 {
351             family inet6 {
352                 address 3040::10/64;
353             }
354         }
355     }
356     xe-0/0/2 {
357         gigether-options {
358             802.3ad ae0;
359         }
360     }
361     xe-0/0/1 {
362         gigether-options {
363             802.3ad ae0;
364         }
365     }
366     ae0 {
367         flexible-vlan-tagging;
368         encapsulation flexible-ethernet-services;
369         aggregated-ether-options {
370             lacp {
371                 active;
372             }
373         }
```

```
374          unit 0 {
375              encapsulation vlan-bridge;
376              vlan-id 1001;
377          }
378      }
379      irb {
380          unit 0 {
381              family inet {
382                  address 30.0.0.3/24;
383              }
384              family inet6 {
385                  address 3010::3/64;
386              }
387          }
388      }
389      lo0 {
390          unit 0 {
391              family inet {
392                  address 3.3.3.3/32;
393              }
394              family inet6 {
395                  address 4001:db8::1/128;
396              }
397          }
398      }
```

Example 5.46 Protocol configuration on R3

```
399      user@R3# show protocols
400      ptp {
401          e2e-transparent;
402      }
403      clock-synchronization {
404          traceoptions {
405              file TCv6;
406              flag all;
407          }
408      }
409      ospf {
410          area 0.0.0.0 {
411              interface irb.0;
412              interface lo0.0;
413          }
414      }
415      ospf3 {
416          area 0.0.0.0 {
417              interface irb.0;
418              interface lo0.0;
419              interface xe-0/0/4.0 {
420                  passive;
421              }
422              interface xe-0/0/3.0 {
423                  passive;
424              }
425          }
426      }
```

Example 5.47 Chassis configuration on R3

```
427      user@R3# show chassis
428      aggregated-devices {
429          ethernet {
430              device-count 10;
431          }
432      }
```

Example 5.48 Configuration of routing-option on R3

```
433      user@R3# show routing-options
434      rib inet6.0 {
435          static {
436              route 3050::15/128 next-hop 3010::101;
437              route 3090::11/128 next-hop 3010::101;
438          }
439      }
440      router-id 3.3.3.3;
```

Example 5.49 Interface configuration on R0

```
441      user@R0# show interfaces
442      xe-0/0/4 {
443          unit 0 {
444              family inet {
445                  address 40.0.0.1/24;
446              }
447              family inet6 {
448                  address 4010::10/64;
449              }
450          }
451      }
452      xe-0/0/3 {
453          unit 0 {
454              family inet {
455                  address 50.0.0.1/24;
456              }
457              family inet6 {
458                  address 5010::10/64;
459              }
460          }
461      }
462      xe-0/0/2 {
463          unit 0 {
464              family inet6 {
465                  address 3090::10/64;
466              }
467          }
468      }
469      xe-0/0/1 {
470          unit 0 {
471              family inet6 {
472                  address 3050::10/64;
473              }
474          }
475      }
476      lo0 {
477          unit 0 {
478              family inet {
479                  address 5.5.5.5/32;
480              }
481              family inet6 {
482                  address 3010::201/128;
483              }
484          }
485      }
```

Example 5.50 Protocol configuration on R0

```
486      user@R0# show protocols
487      ptp {
488          e2e-transparent;
489      }
490      clock-synchronization {
491          traceoptions {
```

```
492                 file TCv6 size 10m;
493                 flag all;
494             }
495         }
496         ospf {
497             area 0.0.0.0 {
498                 interface xe-0/0/4.0;
499                 interface xe-0/0/3.0;
500                 interface xe-0/0/2.0;
501                 interface xe-0/0/1.0;
502                 interface lo0.0;
503             }
504         }
505         ospf3 {
506             area 0.0.0.0 {
507                 interface xe-0/0/4.0;
508                 interface xe-0/0/3.0;
509                 interface xe-0/0/2.0 {
510                     passive;
511                 }
512                 interface xe-0/0/1.0 {
513                     passive;
514                 }
515                 interface lo0.0;
516             }
517         }
```

Example 5.51 Chassis configuration on R0

```
518         user@R0# show chassis
519         aggregated-devices {
520             ethernet {
521                 device-count 1;
522             }
523         }
```

Example 5.52 Configuration of routing-option on R0

```
524         user@R0# show routing-options
525         rib inet6.0 {
526             static {
527                 route 3080::11/128 next-hop 3010::101;
528             }
529         }
530         router-id 5.5.5.5;
```

Summary

This chapter discussed end-to-end deployment of SyncE, the G.8275.1 profile, the G.8275.1.enh profile, the G.8275.2.enh profile, and the Media-profile. TCv6 deployment with MC-LAG and IRB was also discussed. Finally, detailed end-to-end configurations for all of the deployment use cases were provided.

Chapter 6

Performance Measurement

Performance measurement in synchronization is typically a long-term measurement on the characteristics or metrics associated with a clock while operating either as individual node or in a network using a proper reference clock. ITU-T has standardized these metrics as clock specifications and network limits to meet the stringent requirements demanded by the various synchronization applications. Therefore, it is important to qualify these metrics on a given node, as well as on a network, to ensure they comply to the ITU-T recommendation. This chapter specifies the high-level topology and any such limits as per ITU-T recommendation.

NOTE All the performance masks mentioned here are taken from various ITU-T standards mentioned in Chapter 7. Please refer to the respective standard documents for more detailed information.

G.8262/G.8262.1 Clock Specifications

ITU-T G.8262 or the G.8262.1 standard refers to the timing characteristics of a synchronous equipment of client clocks. It mainly covers the clock specifications for Ethernet or Enhanced Ethernet Equipment Clock, respectively. Let's examine the performance metrics and ITU-T mask for the following cases:

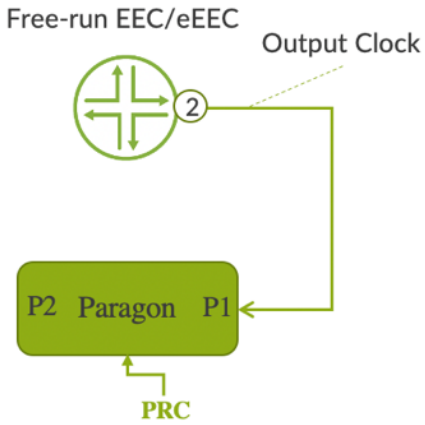
- Free-run accuracy
- Pull-in/hold-in/pull-out range
- Wander generation
- Wander tolerance
- Wander transfer
- Short-term phase transient
- Long-term holdover

Free-run Accuracy

In a free-run case, the device being tested is in free-run mode and measures the output phase wander using a tester which has a stable reference clock. The slope of the time interval error versus observation

interval graph provides the estimate of the free-run accuracy of the clock. The Pass/Fail criteria is $\pm 4.6ppm$. Figure 6.1 shows a typical setup for free-run accuracy validation.

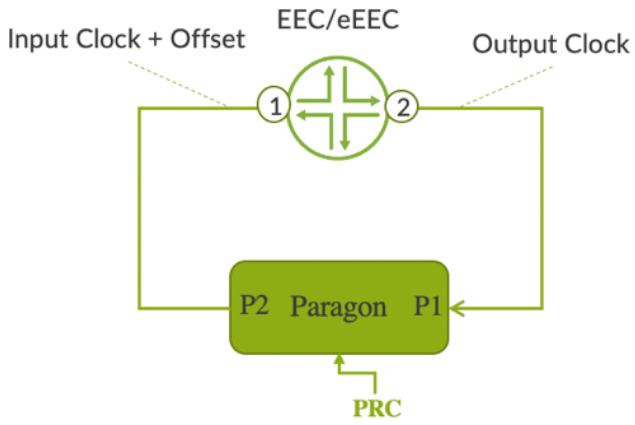
Figure 6.1 G.8262/G.8262.1 Free-run Test Setup



Pull-in/Hold-in/Pull-out Range Test

The setup for pull-in/hold-in/pull-out measurement is shown in Figure 6.2.

Figure 6.2 G.8262/G.8262.1 Pull-in/Hold-in/Pull-out Test Setup



To measure the pull-in range, apply a high frequency offset to the selected clock input using clock tester so that the device will enter into holdover mode. Now reduce the offset in arbitrary small step until EEC/eEEC locks to the input source. EEC/eEEC should lock to the input source before the offset reaches to $\pm 4.6\ ppm$.

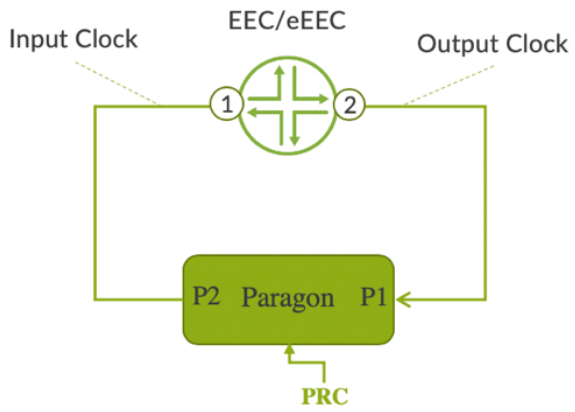
To measure the hold-in range, vary the frequency offset arbitrarily, slowly, and measure the highest frequency offset within which the device maintains lock.

Pull-out range is the offset within which the device stays in locked state and outside of which the device loses the lock irrespective of the rate of the frequency change.

Wander or Noise Generation Test

In wander generation test, the device under test is subject to a wander free clock source such as a SyncE clock from an external clock source, such as the clock tester, and measures the output phase wander noise using the same or different test equipment, which uses the same reference as that of the clock sources.

Figure 6.3 G.8262/G.8262.1 Test Set-up



According to the ITU-T G.8262/G.8262.1 specifications, the output wander under normal locked mode of EEC and enhanced EEC should satisfy the MTIE and TDEV requirements as depicted in Figure 6.4 through Figure 6.9. Wander generation test is typically performed in an observation window of a minimum 3000sec. Separate limits are defined for variable temperature. However, in this book, you will see only the measurements applicable to constant temperature (+/-1K).

Figure 6.4 G.8262 EEC Opt.1 Wander Gen Const. Temp (MTIE)

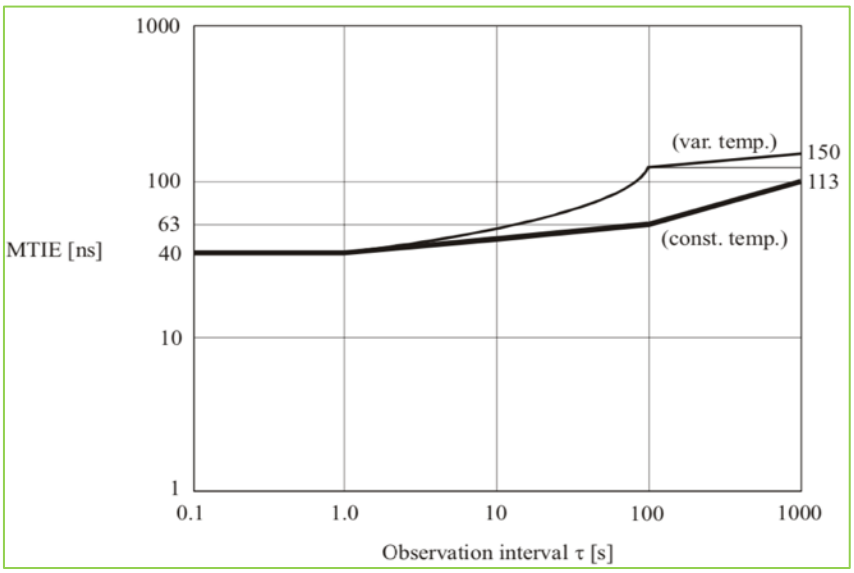


Figure 6.5 G.8262.1 eEEC Wander Gen Const. Temp (MTIE)

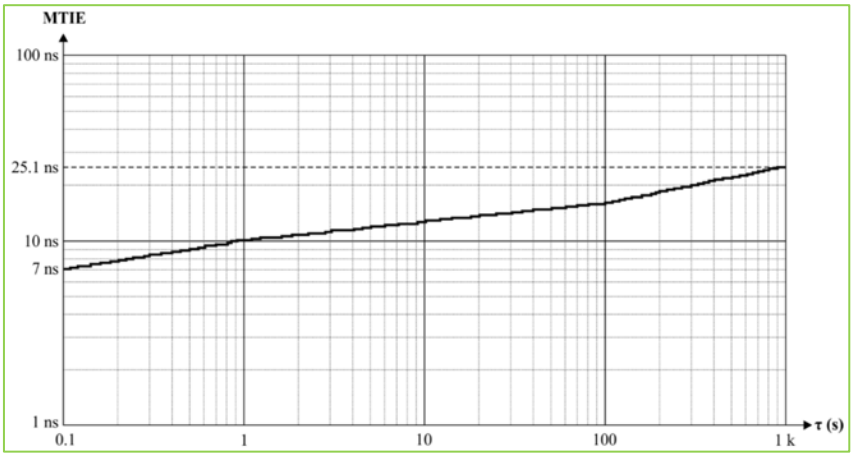


Figure 6.6 G.8262 EEC Opt.1 Wander Gen Const. Temp (TDEV)

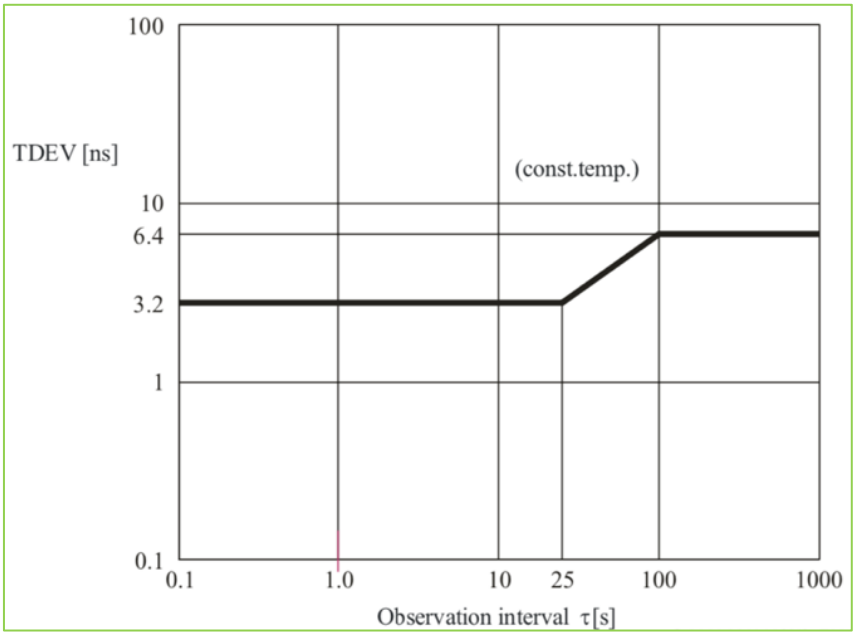


Figure 6.7 G.8262.1 eEEC Wander Gen Const. Temp (TDEV)

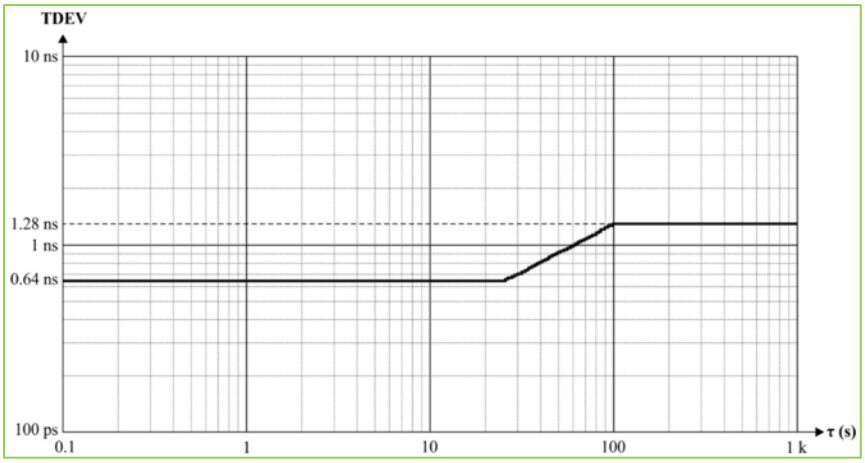


Figure 6.8 G.8262 EEC Opt.2 Wander Gen Const. Temp (MTIE)

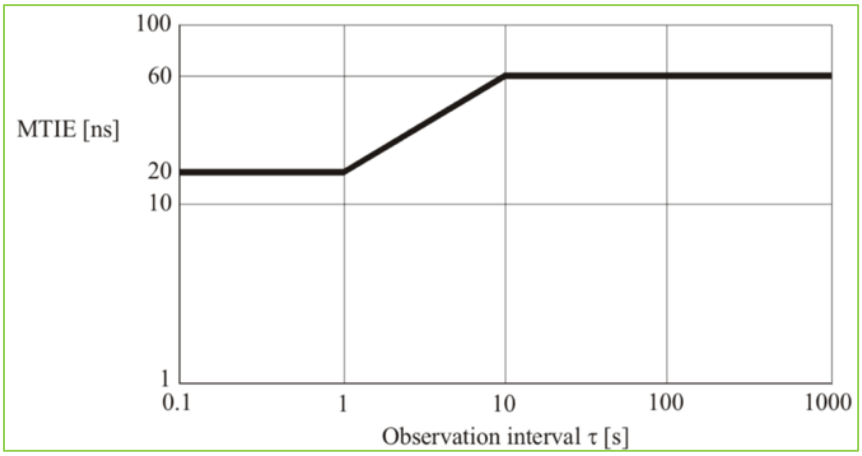
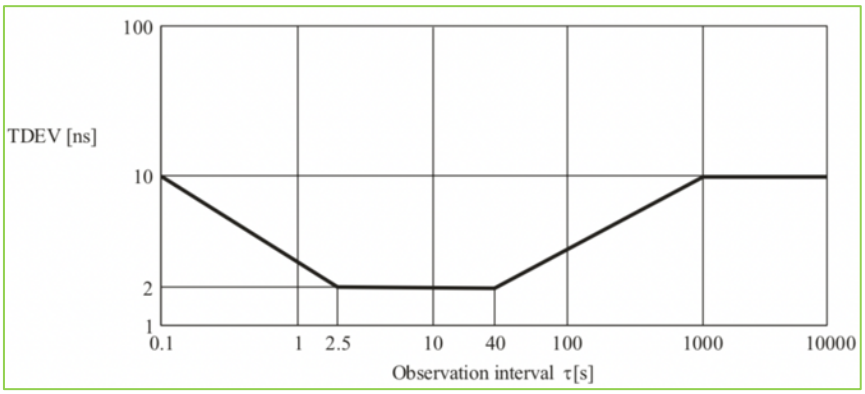


Figure 6.9 G.8262 EEC Opt.1 Wander Gen Const. Temp (TDEV)



Wander/Noise Tolerance (Option 1)

The wander tolerance test is to verify the wander noise handling capability of the device under test. The device is initially locked to a wander free signal and after the pre-stabilization period, wander impairment is added to the device as per the input wander tolerance expressed in MTIE and TDEV limits, as shown in Figures 6.10 through Figure 6.12. There is no output noise requirement for noise tolerance. Rather, the criteria below are defined for the device under test:

- Not causing any alarms,
- Not causing the clock to switch reference, and
- Not causing the clock to go into holdover.

Figure 6.10 G.8262 EEC Opt.1 Input Wander Limit (MTIE)

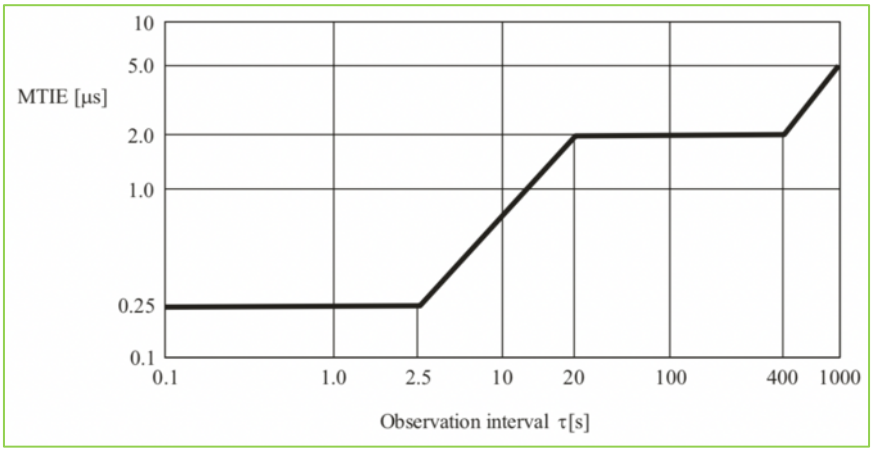
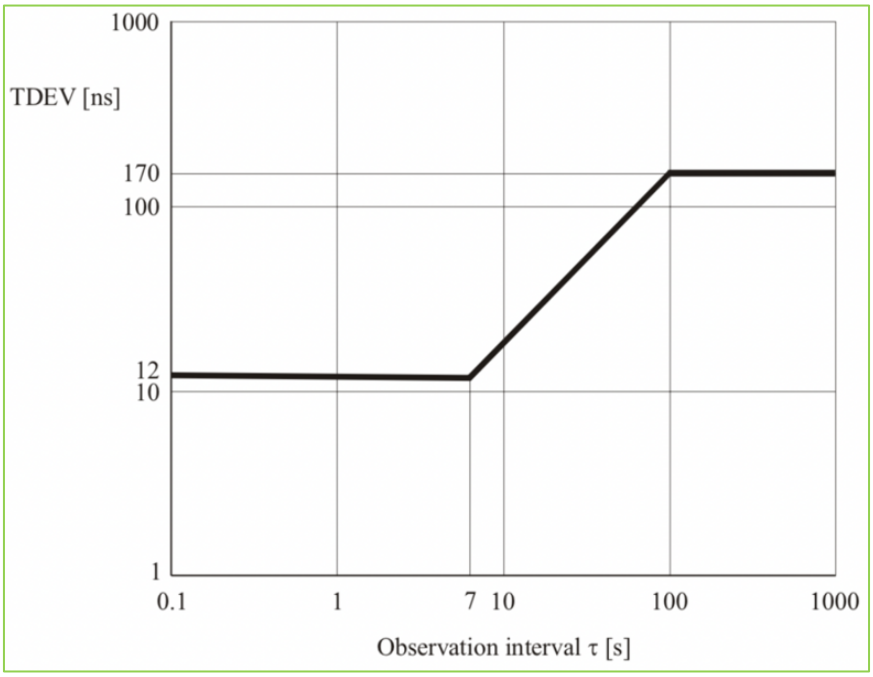


Figure 6.11 G.8262 EEC Opt.1 Input Wander Limit (TDEV)

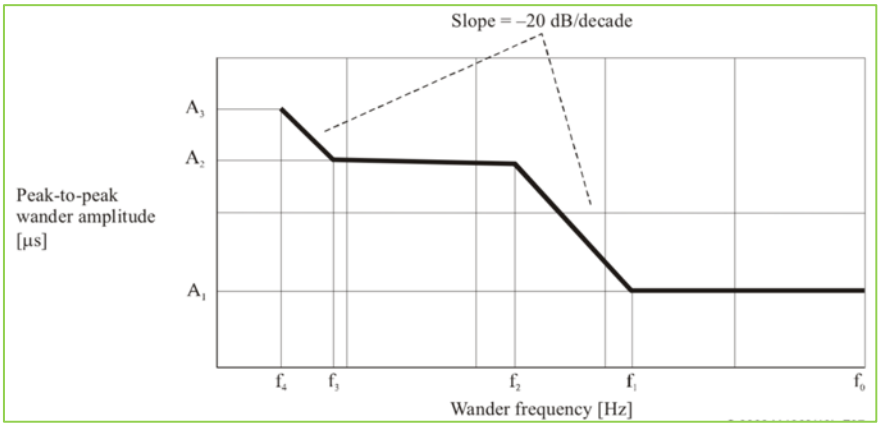


The following frequencies and corresponding amplitudes are constructed from the above masks for application at the input of the device under test.

Table 6.1 Wander amplitude of frequency tones-Opt-1

Peak-to-peak wander amplitude			**Wander frequency**				
A_1 [µs]	A_2 [µs]	A_3 [µs]	f_4 [mHz]	f_3 [mHz]	f_2 [mHz]	f_1 [Hz]	f_0 [Hz]
0.25	2	5	0.32	0.8	16	0.13	10

Figure 6.12 G.8262 EEC Opt.1 Input Wander Tolerance Lower Limit



Wander Tolerance (Option-2)

The wander tolerance Option 2 is defined for TDEV only. There is no peak wander tolerance specification for the Option 2 clock. Hence SyncE uses the MTIE wander limit of 1.544kbps signal for deriving the frequency tones as shown in Figure 6.13. Since the TDEV mask only goes up to 1000sec, the maximum observation interval in the Table 6.2 is set to 1000sec.

Figure 6.13 G.8262 EEC Opt.2 Input Wander Limit (MTIE)

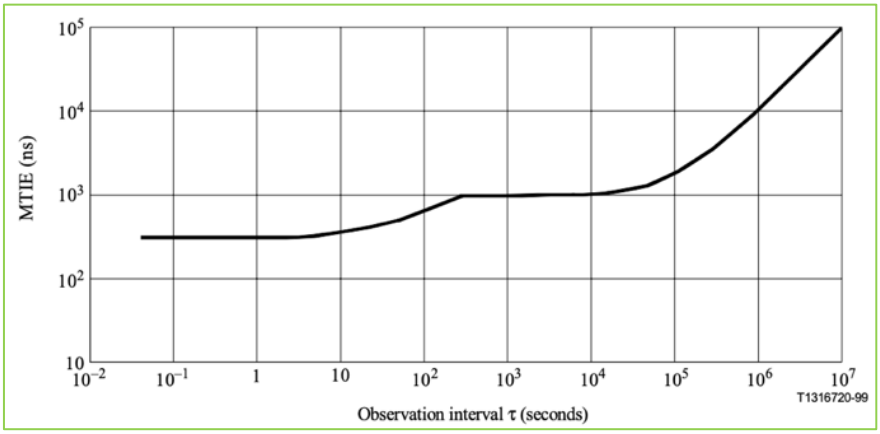
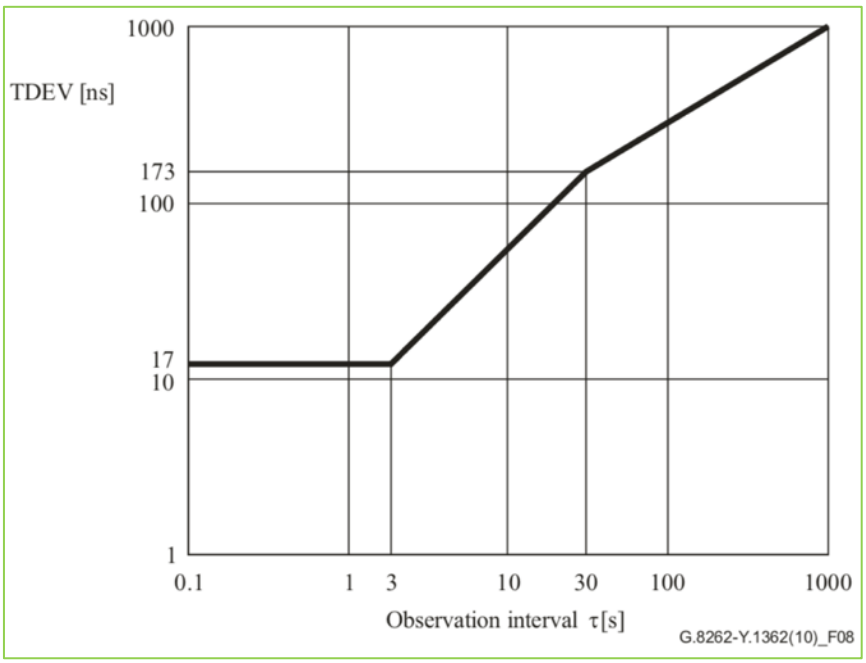


Table 6.2 Wander amplitude of frequency tones-Opt-2

Observation Interval (s)	MTIE (ns)	Tone Frequency (Hz)	Tone Amplitude (ns)
0.1	300	3.2	300
1	303	0.32	303
10	325	0.032	325
100	550	0.0032	550
280	1000	0.0011	1000

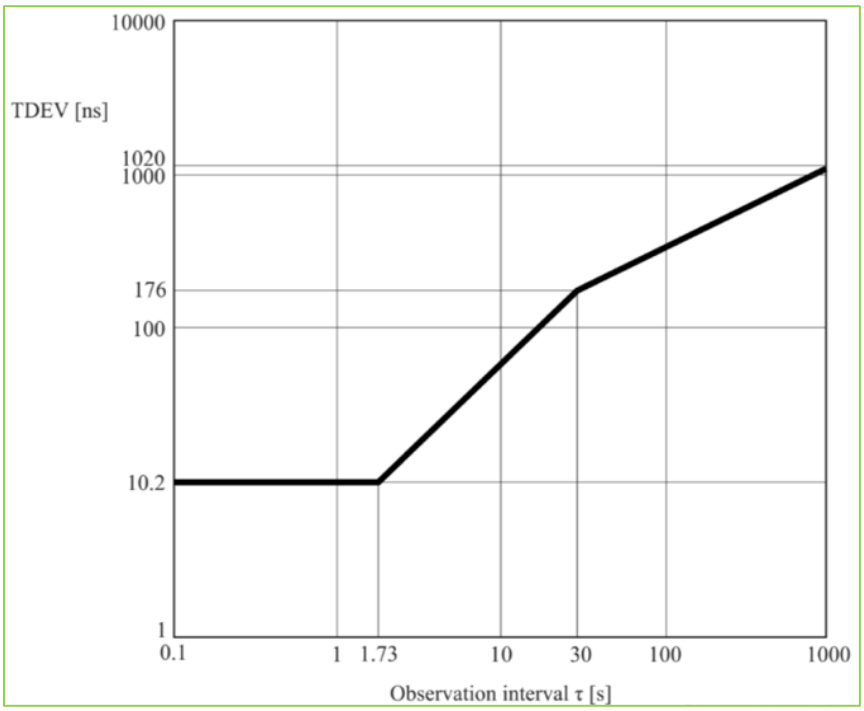
1000	**1010**	**0.00032**	**1010**

Figure 6.14 G.8262 EEC Opt.2 Input Wander Limit (TDEV)



It is important to note that there is output mask defined for wander tolerance for Option 2 TDEV as in Figure 6.15.

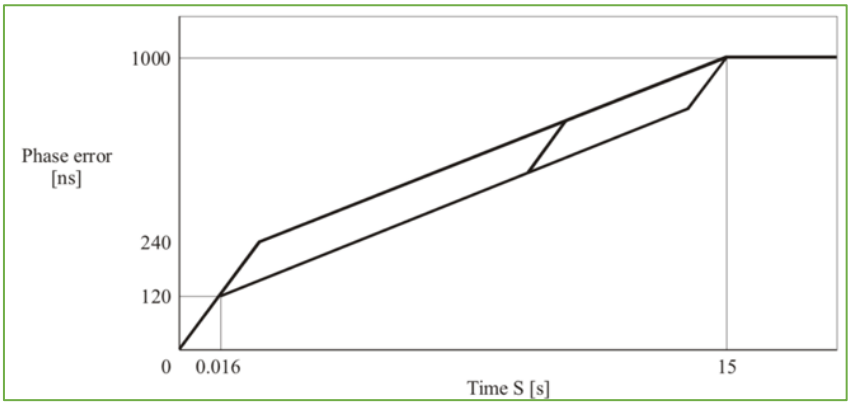
Figure 6.15 G.8262 EEC Opt.1 Max. Output Wander Limit (TDEV)



Short-term Phase-transient – Option 1

The short-term phase-transient requirement reflects the performance of the clock, when the selected input reference is lost and a second reference input signal, traceable to the same reference clock, is available simultaneously, or shortly after the detection of the failure. In such cases, the reference is lost for at most 15 seconds. The output phase variation should meet the mask defined in Figure 6.16.

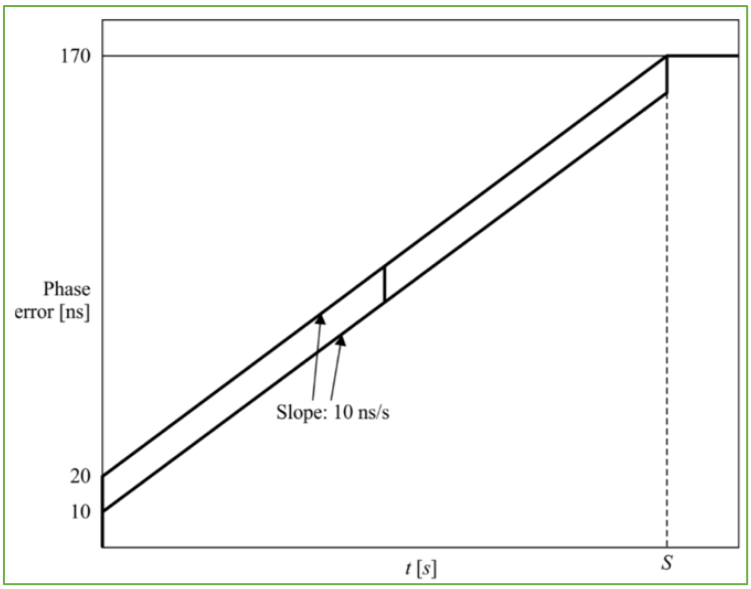
Figure 6.16 G.8262 EEC Opt.1 Max Output Phase Transient



In Figure 6.16, the first jump indicates the loss of input reference and the EEC moves to holdover. The second jump, which is to take place within 15 seconds after entering holdover, accounts for the switching to the secondary reference. The overall output phase error should remain constant and smaller than 1µs.

In Figure 6.17, when the active/selected input reference is lost, the eEEC enters into the holdover state. This is indicated by the first jump of 10ns.

Figure 6.17 G.8262.1 eEEC Opt.1 Max Output Phase Transient

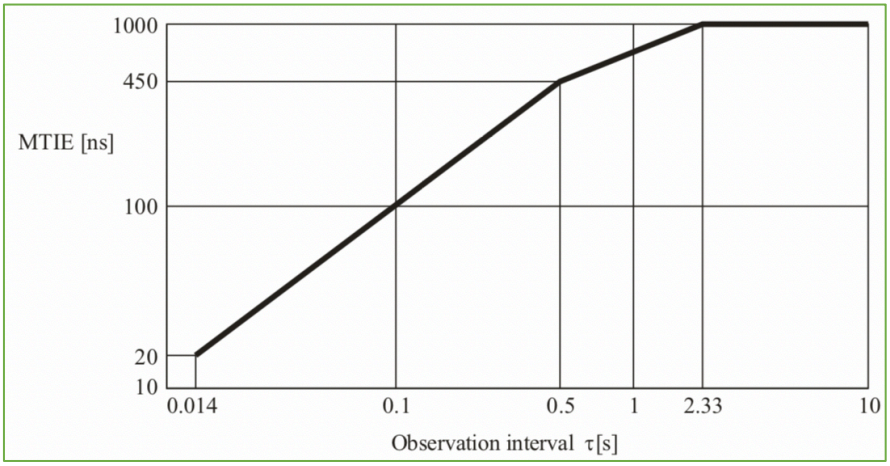


In the holdover state, the phase error is restricted to 10 ns/s. When a second reference input signal is available and qualified, the eEEC switches to the second reference. This is represented by the second jump of 10 ns. The overall output phase error should remain constant and smaller than 170 ns.

Short-term Phase-transient – Option 2

The phase transient at the output of Option 2, in cases of rearrangement should meet the following MTIE mask.

Figure 6.18 G.8262 EEC Opt. 2 Max Output Phase Transient



Long-term Phase-transient (Option 1)

The long-term phase-transient is defined for a period of more than 15 seconds subject to a limit with maximum frequency offset of +/-4.6ppm. The output phase error of EEC and eEEC during holdover mode is illustrated by Figures 6.19 and 6.20.

Figure 6.19 G.8262 EEC Opt.1 Output Phase Error Holdover Const Temp

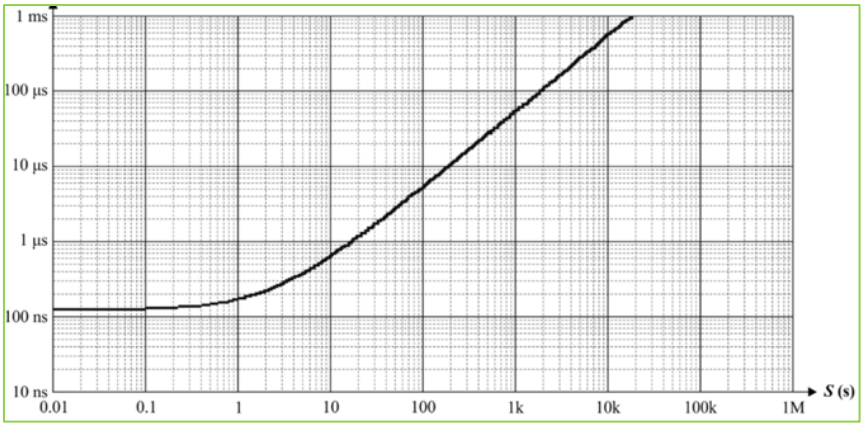
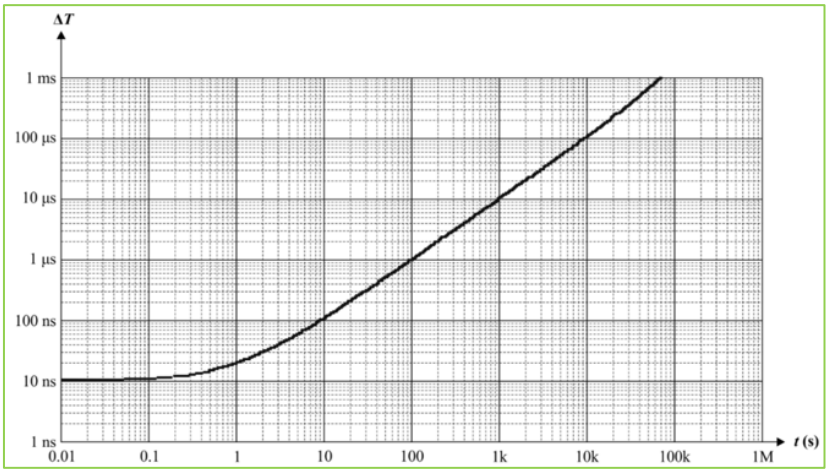


Figure 6.20 G.8262.1 eEEC Opt.1 Output Phase Error Holdover Const Temp



G.8263 Clock Specifications

The ITU-T G.8263 refers the clock specifications of the Packet Equipment Client Clock (PEC-S). This specification is used when the PEC-S is used with G.8265.1 profile. You will see the following clock specifications:

- Frequency accuracy,
- Noise generation, and
- Noise tolerance.

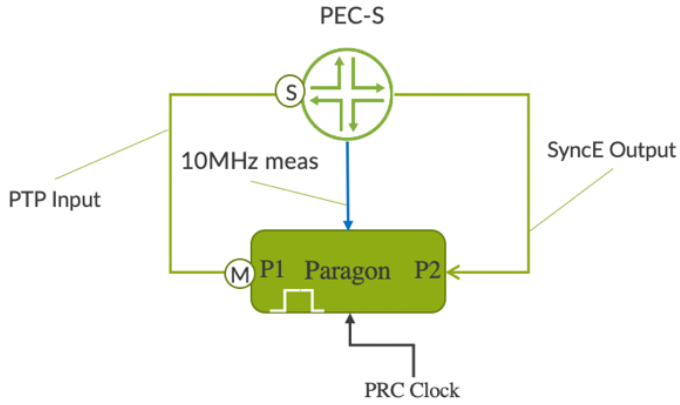
Frequency Accuracy

Under Free running conditions, the output frequency accuracy of PEC-S shouldn't be greater than 4.6 PPM with reference to a stable G.811 clock.

Noise Generation Test

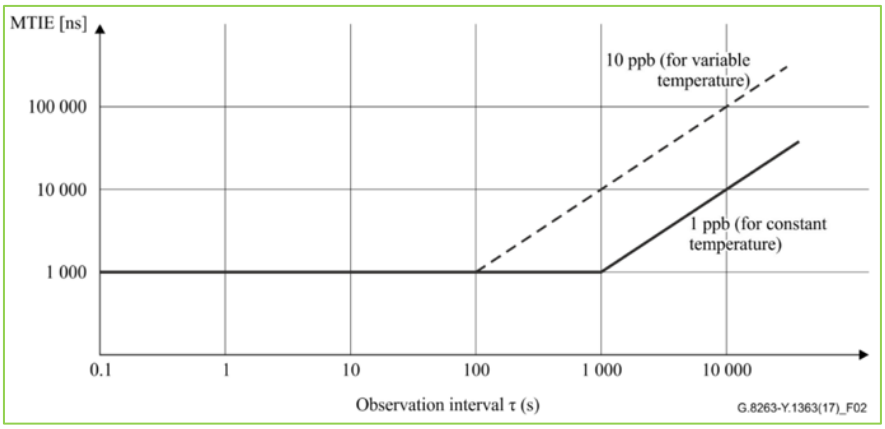
Figure 6.21 is used for Noise-generation measurement for PEC-S clock. The tester is given a PRC reference clock and it measures the output wander noise at P2.

Figure 6.21 G.8263 PEC-S Wander Generation



The output phase noise of a PEC-S clock when an ideal input reference packet timing signal (PTS) is provided by the following MTIE mask.

Figure 6.22 G.8263 PEC-S Wander Generation



Noise Tolerance Test

The noise tolerance limit to PEC-S is based on the ITU-T G.8261.1 network limits mentioned in Figure 6.49. The criteria below are defined for the device under test. It should:

- not cause the packet timing signal fail;
- not cause the clock to go into holdover, and;
- maintain the clock within the following prescribed performance limits, depending on the applicable use case:
  - the limits as per ITU-T G.8261.1 at reference point D.

G.8273.2 Clock Specifications

ITU-T G.8273.2 refers to the clock specifications of the T-BC and T-TSC clock. Let's discuss the following performance specifications of the G.8273.2 clock:

- Noise generation
- Noise tolerance
- Noise transfer
- Phase transient
- Holdover

Noise Generation Test

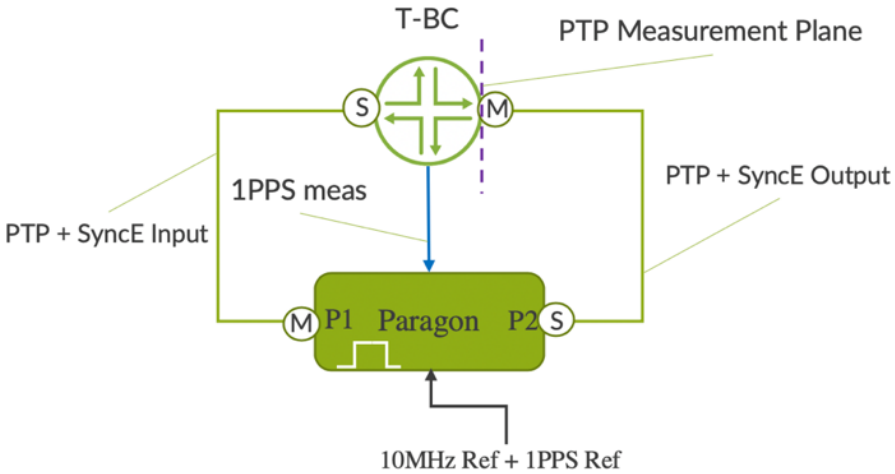
As mentioned in Figure 6.23, in the noise generation test, the device under test is given a noise free PTP and SyncE clock at its input and measures the output noise on SyncE, PTP, and 1PPS clock using the clock tester. In this case the tester should have a proper 10MHz and 1PPS reference. As mentioned here,it is important to compensate the cable length to get the desired results:

- Cable that connects the master port of T-BC to tester client port.
- 1PPS measurement cable from DUT to clock tester.
- 1PPS reference cable to the clock tester.

NOTE Cable compensation of 5.1nsec per meter for electrical cable and 4.9nsec per meter for optical cable is recommended.

NOTE The ITU-T G.8271 indicated that there is a 10nsec uncertainty associated with the rising edge of the 1PPS pulse. So it is important that the termination impedance is correctly matched to the cable impedance. This will otherwise degrade the rising edge of signal, leading to further significant measurement uncertainty. The recommendation is to use signals with 50ohms cable termination.

Figure 6.23 G.8273.2 Test Setup



SyncE performance should meet the ITU-T G.8262/G.8262.1 clock specifications. Refer to the previous sections in this chapter for details. The packet level performance should meet the metrics in Table 6.3, based on the device capability. ITU-T has classified four classes of T-BC/T-TSC: Class-A, Class-B, Class-C, and Class-D. The performance metrics of Class-D is for further study (FFS) except for the Max TE-LPF. Similarly, the 1PPS performance should meet the metrics as per Table 6.4.

Table 6.3 G.8273.2 Packet Performance Metrics

		Class-A	Class-B	Class-C	Class-D
Max Time Error-2WAY (|Max TE|)	METRICS	100ns	70ns	30ns	FFS
Max Time Error LPF-2WAY (|Max TEL|)		--	--	--	5ns
Constant Time Error-2WAY (cTE-2WAY)		±50ns	±20ns	±10ns	FFS
Constant Time Error-T1 (cTE T1)		±50ns	±20ns	±10ns	FFS
Constant Time Error-T4 (cTE T4)		±50ns	±20ns	±10ns	FFS
Dynamic Time Error-HF (dTE-HF)		70ns	70ns	30ns	FFS
Dynamic Time Error-LF (dTE-LF)		40ns	40ns	10ns	FFS
Dynamic MTIE-LF (dMTIE-LF)		40ns (Mask)	40ns (Mask)	10ns (Mask)	FFS
Dynamic TDEV-LF (dTDEV-LF)		4 ns (Mask)	4 ns (Mask)	2ns (Mask)	FFS

Table 6.4 G.8273.2 Performance Metrics-1PPS

		Class-A	Class-B	Class-C
1PPS Time Error (|1PPS TE|)	METRICS	100ns	70ns	30ns
1PPS Constant Time Error (1PPS cTE)		±50ns	±20ns	±10ns
Dynamic Time Error-HF (dTE-HF)		70ns	70ns	30ns
Dynamic Time Error-LF (dTE-LF)		40ns	40ns	10ns
Dynamic MTIE-LF (dMTIE-LF)		40ns (Mask)	40ns (Mask)	10ns (Mask)
Dynamic TDEV-LF (dTDEV-LF)		4ns (Mask)	4ns (Mask)	2ns (Mask)

The ITU-T G.8273.2 specifies the noise generation of a pair of T-BCs as listed in Table 6.5.

Table 6.5 Time Error Metrics of a Pair of T-BCs

	Class-A		Class-B		Class-C	
	1xT-BC	**2xT-BC**	**1xT-BC**	**2xT-BC**	**1xT-BC**	**2xT-BC**
cTE (ns)	**±50**	**±100**	**±20**	**±40**	**±10**	**±20**
dTEL MTIE (ns)	**40**	**60**	**40**	**60**	**10**	**15**
dTEL TDEV (ns)	**4**	**6**	**4**	**6**	**2**	**3**
dTEH (peak-to-peak, ns)	**70**	**70**	**70**	**70**	**30**	**30**
Max |TE| (ns)	**100**	**160**	**70**	**100**	**30**	**45**

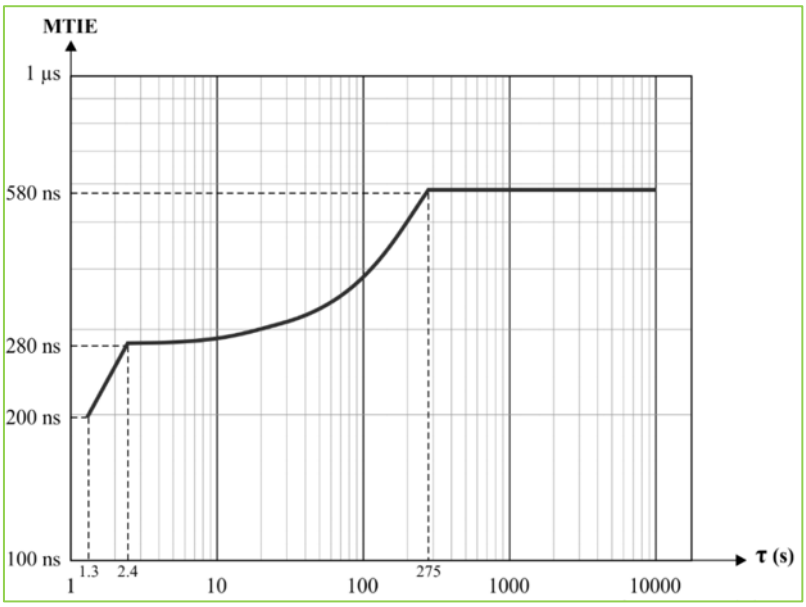
Noise Tolerance Test

Refer to the topology in Figure 6.23. A noise tolerance test for T-BC in hybrid mode involves applying a G.8273.2 noise pattern and a G.8262 or G.8262.1 noise pattern simultaneously at the input of T-BC, and verifying that T-BC satisfies the following conditions:

- Not causing any alarms,
- Not causing the clock to switch reference, and
- Not causing the clock to go into holdover.

The G.8273.2 noise pattern is based on the G.8271.1 network limit for dTE as shown in Figure 6.24.

Figure 6.24 G.8273.2 Input Noise Pattern



Noise Transfer for T-BC

Refer to the topology in Figure 6.23 for the noise transfer measurement. Noise transfer of a clock refers to the transfer of time error from PTP input interface to the PTP and 1PPS output interfaces and the transfer of phase wander from SyncE input to the SyncE, PTP, and 1PPS output interfaces.

- PTP to PTP/1PPS noise transfer
- SyncE to SyncE noise transfer
- SyncE to PTP/1PPS noise transfer

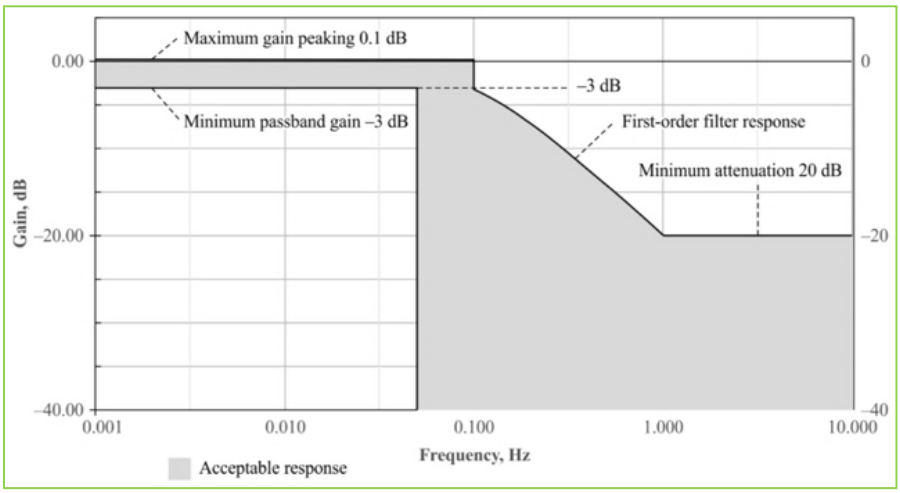
Noise Transfer is usually expressed in terms of the filter bandwidth of the clock as specified in Table 6.6.

Table 6.6 G.8273.2 Noise-transfer Function

Input	Output	Transfer Function
PTP	**PTP**	**0.05 to 0.1 Hz LPF**
PTP	**1PPS**	**0.05 to 0.1 Hz LPF**
SyncE (G.8262)	**SyncE (G.8262)**	**1 to 10Hz LPF**
SyncE (G.8262.1)	**SyncE (G.8262.1)**	**1 to 3Hz LPF**
SyncE (G.8262)	**PTP**	**[0.05 to 0.1 Hz; 1 to 10 Hz] BPF**
SyncE (G.8262)	**1PPS**	**[0.05 to 0.1 Hz; 1 to 10 Hz] BPF**
SyncE (G.8262.1)	**PTP**	**[0.05 to 0.1 Hz; 1 to 3 Hz] BPF**
SyncE (G.8262.1)	**PTP**	**[0.05 to 0.1 Hz; 1 to 3 Hz] BPF**

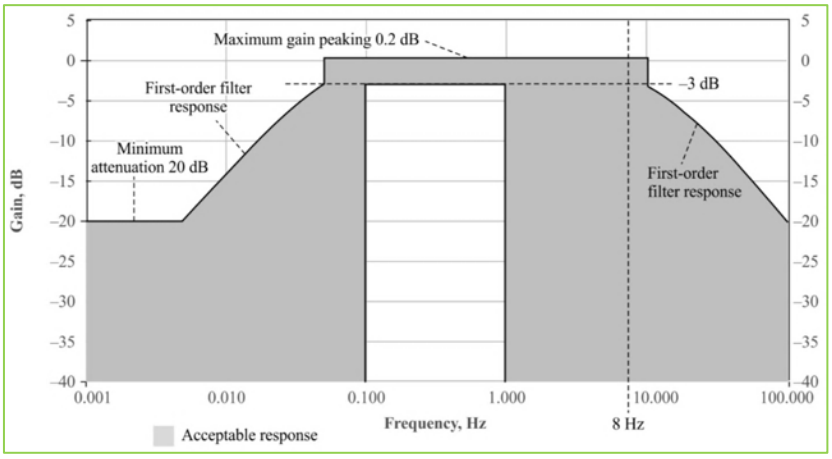
The frequency response of the acceptable PTP to PTP/1PPS filter implementation of T-BC as per the ITU-T G.8273.2 is depicted in Figure 6.25.

Figure 6.25 Frequency Response of PTP to PTP/1PPS Filter



And the frequency response of the acceptable SyncE to PTP/1PPS filter implementation of T-BC as per ITU-T G.8273.2 is depicted in Figure 6.26.

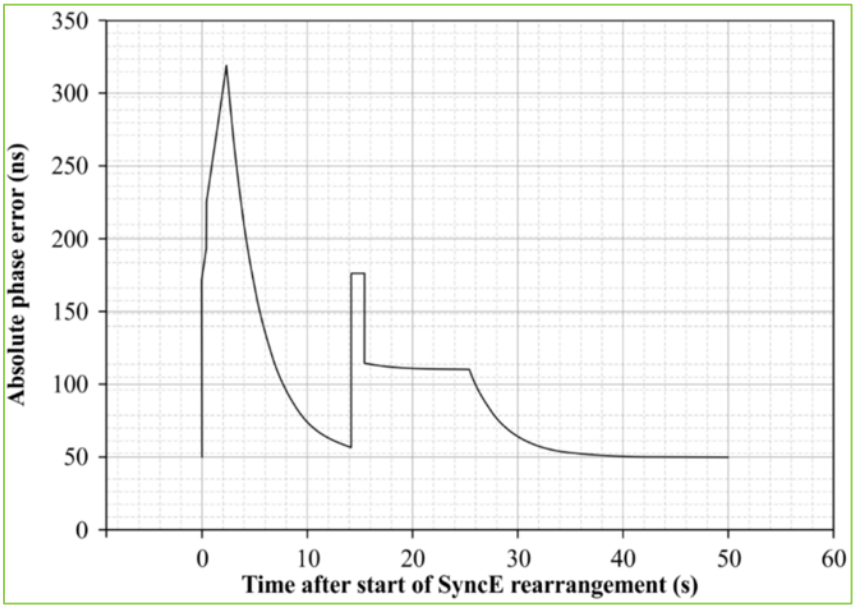
Figure 6.26 Frequency Response of SyncE to PTP/1PPS Filter



Phase Transient Due to SyncE Rearrangements

Refer back to Figure 6.23 for verifying the phase transient. The maximum allowable phase/time error at the output of T-BC due to the SyncE rearrangements is shown in Figure 6.27.

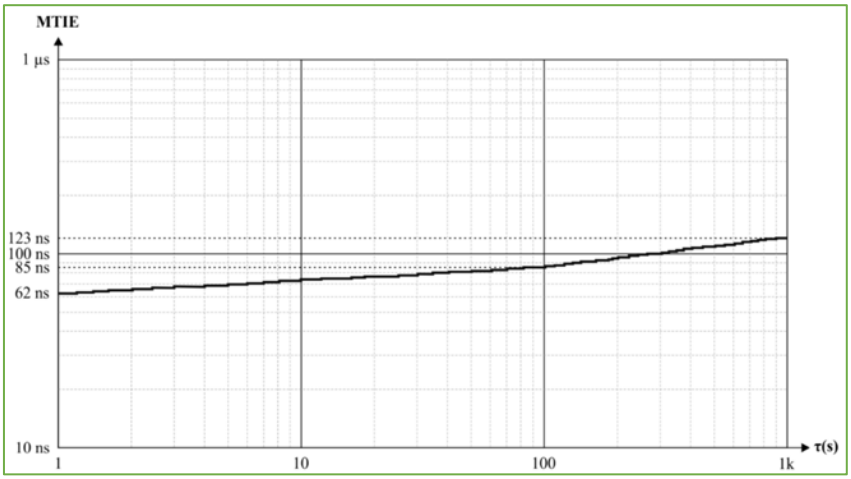
Figure 6.27 G.8273.2 T-BC Output Phase for SyncE Transient



Holdover with Support of Physical Layer Frequency

The allowable phase error, when a T-BC enters in phase/time holdover with support of physical layer SyncE at constant temperature, is shown in Figure 6.28. This has been defined for Class-A/Class-B devices. This type of holdover is called *assisted holdover*.

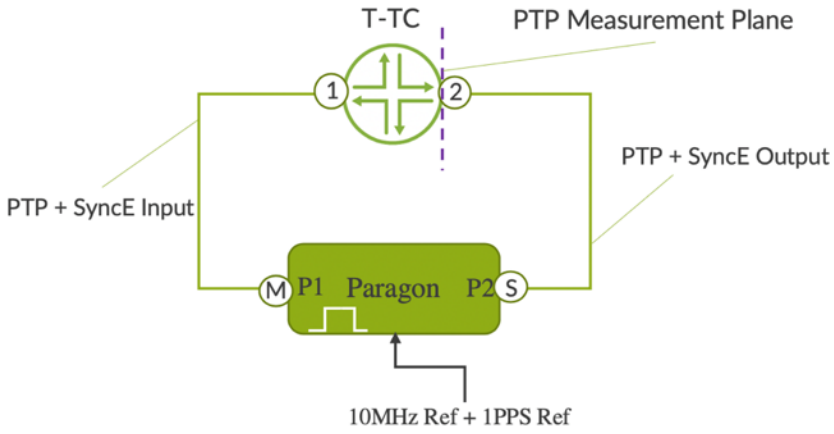
Figure 6.28 G.8273.2 T-BC Loss of PTP Input Const. Temp (MTIE)



G.8273.3 Clock Specifications

The G.8273.3 define the clock specifications of syntonized transparent clock or Telecom Transparent Clock (T-TC). Figure 6.29 below depicts the setup for Time Error measurements for T-TC.

Figure 6.29 G.8273.3 T-TC Test Setup



For transparent clock testing, the clock tester can be configured in either BC or TC mode. Apply a noise-free PTP and SyncE at the input of TC and measure the output noise using the same tester. It is important to compensate the cable length to get the desired result:

- Cumulative cable length of the cable that connects the master port of tester to xe-0/0/1 of T-TC and that connects the xe-0/0/2 of T-TC to tester client port P2, and
- 1PPS reference cable to the tester.

Table 6.7 shows the expected performance metrics of T-TC.

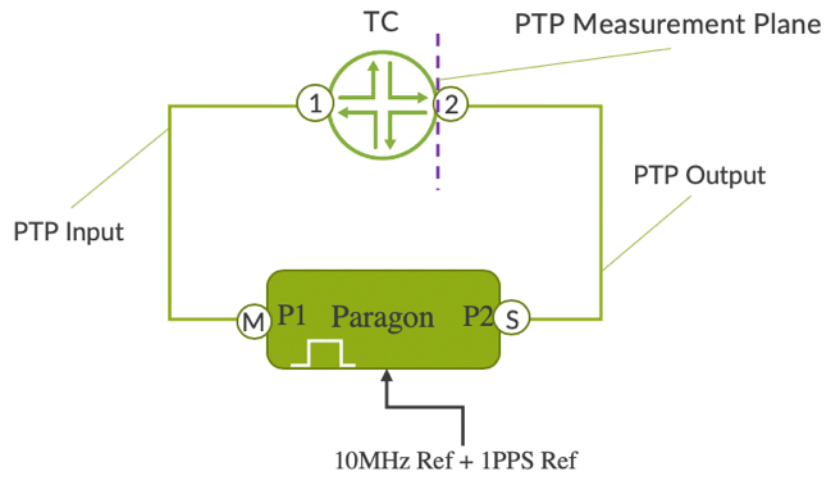
Table 6.7 G.8273.3 Performance Metrics

		Class-A	Class-B
Max Time Error-2WAY (|Max TE|)	METRICS	100ns	70ns
Constant Time Error-2WAY (cTE-2WAY)		±50ns	±20ns
Constant Time Error-T1 (cTE T1)		±50ns	±20ns
Constant Time Error-T4 (cTE T4)		±50ns	±20ns
Dynamic Time Error-HF (dTE-HF)		70ns	70ns
Dynamic Time Error-LF (dTE-LF)		40ns	20ns
Dynamic MTIE-LF (dMTIE-LF)		40ns (Mask)	20ns (Mask)
Dynamic TDEV-LF (dTDEV-LF)		4ns (Mask)	4ns (Mask)

However, TC can be made to operate without the physical layer SyncE. It uses the onboard oscillator clock for synchronizing the PHY counter. Figure 6.30 depicts a normal TC without any SyncE assist.

NOTE For TC, the measurements are carried out for various port speed combinations and traffic with symmetric and asymmetric load with varying packet size.

Figure 6.30 TC Test Setup



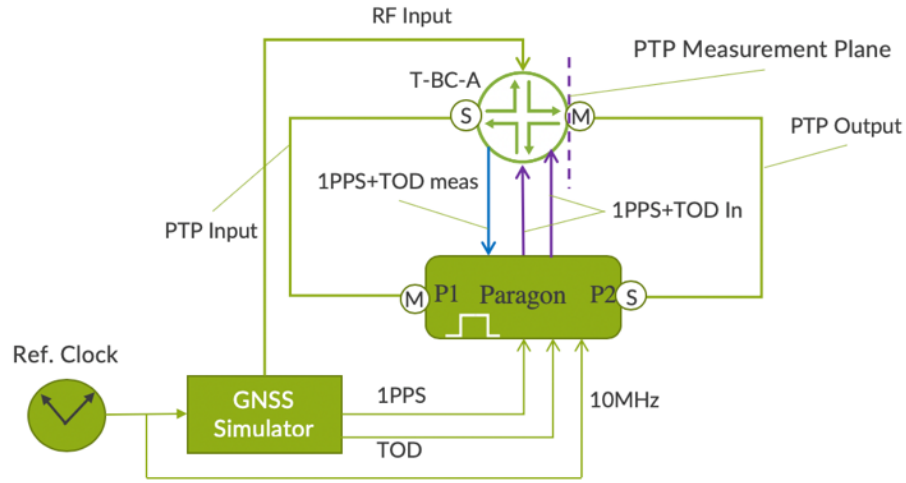
G.8273.4 Clock Specifications

G.8273.4 defines the clock specifications of assisted partial timing T-BC-A/T-TSC-A clock and partial timing T-BC-P/T-TSC-P clock.

Noise Generation Test T-BC-A

Noise generation of a T-BC-A represents the amount of noise produced at the output when there is an ideal input reference packet timing signal.m. The maximum absolute time error at the output of T-BC-A with integrated GNSS as the timing input is 100ns greater than it would be in the case with external timing reference such as 1pps.

Figure 6.31 G.8273.4 T-BC-A Test Setup



The permissible range of cTE and dTEL is defined in Table 6.8.

NOTE Estimate of cTE measurements should be carried out for an averaging window of size at least 10,000 seconds. Also the Ref.Clock should be G.811 PRC.

Table 6.8 G.8273.4 T-BC-A Performance Metrics

	Input	cTE	dTEL
Class-A	GNSS	Not defined	Not defined
	1PPS	±50 ns	50 ns p-p
	PTP	Not defined	200 ns p-p
Class-B	GNSS	Not defined	Not defined
	1PPS	±20 ns	50 ns p-p
	PTP	Not defined	200 ns p-p

Noise Tolerance Test T-BC-A

Refer the topology in Figure 6.31. Noise tolerance test for T-BC-A involves applying a G.8271.2 noise pattern at the input of T-BC-A and verifying that T-BC-A satisfies the following conditions:

- Not causing any alarms,
- Not causing the clock to switch reference,
- Not causing the clock to go into holdover, and
- Maintaining the maximum absolute time error at its 1PPS output that should be below 1.35usec.

Short-term Phase Transient

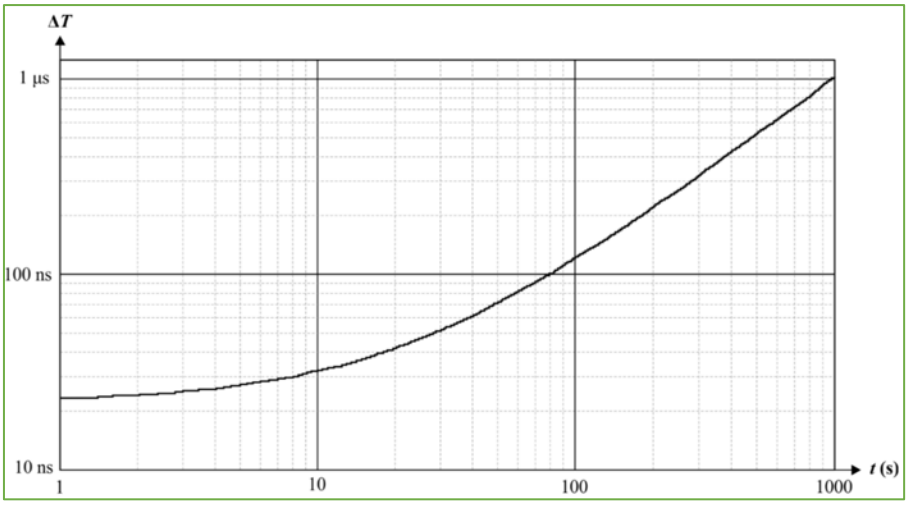
The short-term phase transient of PTP and 1PPS output due to loss and restoration of local time reference (1PPS) input is as follows:

- The transient response due to the loss of the local time reference shall be less than 22ns MTIE.
- The period of loss of the local time reference while in holdover shall comply Figure 6.32.
- The transient response due to the restoration of the local time reference shall be less than 22 ns MTIE.

Holdover of T-BC-A Using Local Oscillator

When the ideal local time reference is disconnected and the backup PTP source is not available, the T-BC-A or T-TSC-A enters the holdover state. The permissible limit of output phase error of T-BC-A or T-TSC-A under holdover at constant temperature is represented in Figure 6.32.

Figure 6.32 G.8273.4 T-BC-A Holdover Performance



Holdover of T-BC-A based on PTP

The phase/time performance during loss of the local time reference based on available PTP input to T-BC-A or T-TSC-A under constant temperature is within 222 nsec for an observation period of 1000 sec, where 200 nsec comes from the noise-generation of the EEC when locked to PTP input.

Noise Generation Test T-BC-P

Figure 6.33 G.8273.4 Noise Generation Test Setup

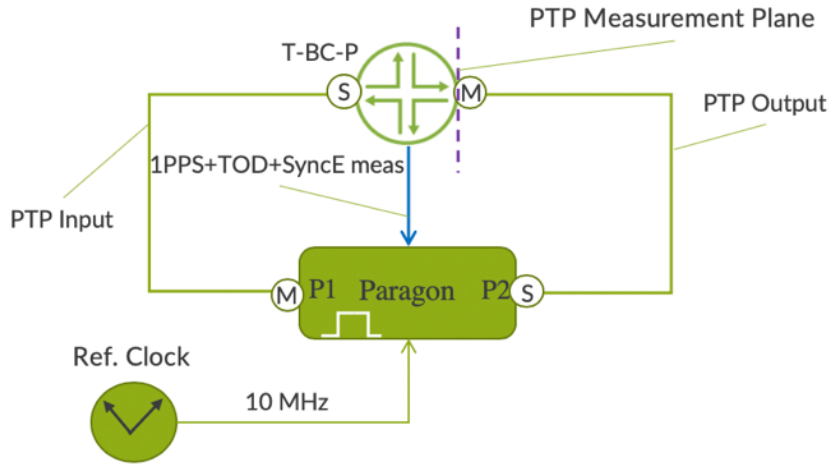


Table 6.9 G.8273.4 T-BC-P Performance Metrics

	Input	cTE	dTEL
Class-A	PTP	±50 ns	200 ns p-p
Class-B	PTP	±20 ns	200 ns p-p

Noise Tolerance Test T-BC-P

Refer to the topology in Figure 6.33. The noise tolerance test for T-BC-P involves applying a G.8271.2 noise pattern at the input of T-BC-P and verifying that T-BC-P satisfies the following conditions:

- Not causing any alarms,
- Not causing the clock to switch reference,
- Not causing the clock to go into holdover, and
- Maintaining the maximum absolute time error at its 1PPS output should be below 1.35usec.

Short-term Phase Transient of T-BC-P

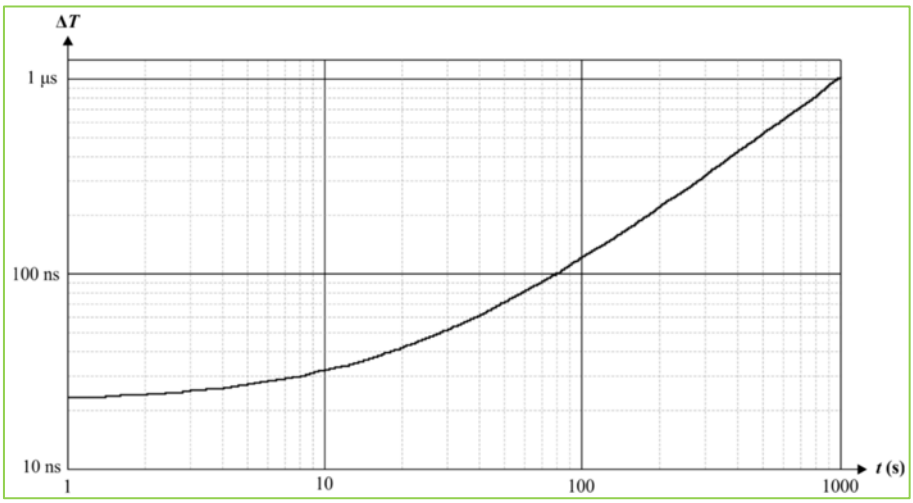
The short-term phase transient of PTP and 1PPS output due to loss and restoration or switching of PTP input is as follows:

- The transient response due to the loss of PTP reference shall be less than 22ns maximum time interval error (MTIE).
- The period of loss of PTP while in holdover shall comply with Figure 6.34.
- The transient response due to the restoration of PTP shall be less than 22ns MTIE.

Holdover Test T-BC-P

The phase/time performance during loss of the PTP input based on a local oscillator applicable to a T-BC-P or T-TSC-P is shown in Figure 6.34.

Figure 6.34 G.8273.4 T-BC-P Holdover Performance



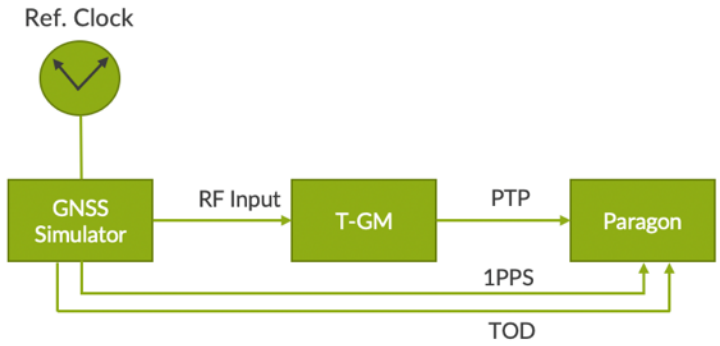
Holdover of T-BC-P using Physical Layer Frequency

When a T-BC-P or T-TSC-P loses all of its input phase and time references, it enters the phase/time holdover state. Under these circumstances, the T-BC-P or T-TSC-P may rely on a physical layer frequency assistance reference traceable to a primary reference clock (PRC). The requirement is same as that of T-BC as per G.8273.2 as mentioned in Figure 6.28.

G.8272 Clock Specifications

Figure 6.35 depicts the G.8272 T-GM setup for measuring the time error and wander generation metrics for MTIE and TDEV.

Figure 6.35 G.8272 T-GM Test Setup



RF output from a GNSS simulator is fed to the T-GM and measures the time and wander using a tester, which uses 1PPS and TOD signal from the GNSS simulator. Figures 6.36 and Figure 6.37 show the MTIE and TDEV limit of the output phase wander.

Figure 6.36 G.8272 PRTC Wander Gen (MTIE)

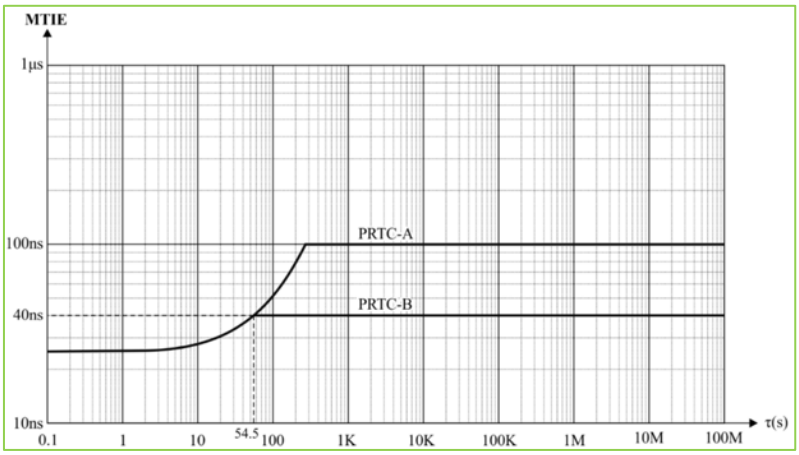
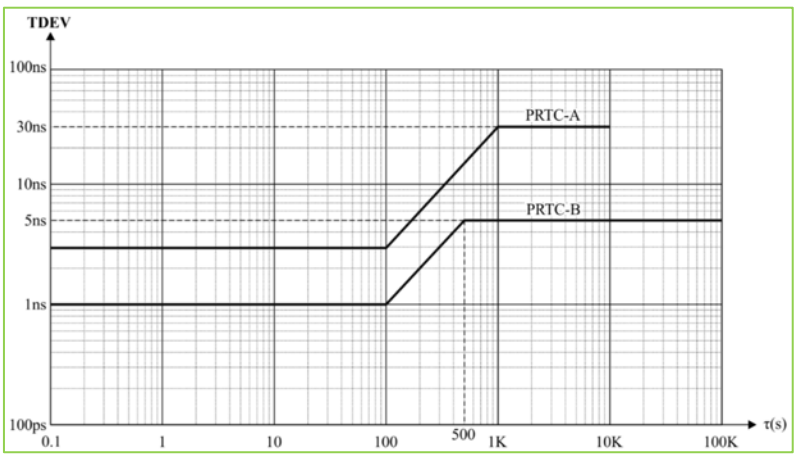


Figure 6.37 G.8272 PRTC Wander Gen (TDEV)



G.8261 Network Limits

G.8261 defines the timing and synchronization aspect in packet networks. It specifies the network limit of SyncE and CES enabled networks.

Network Wander Limit

The network wander limit is typically characterized by MTIE and TDEV. The network limits of a chain of EECs at the measurement plane B in Figure 6.38 is mentioned in Figures 6.39 through 6.43.

Figure 6.38 G.8261 Test Setup

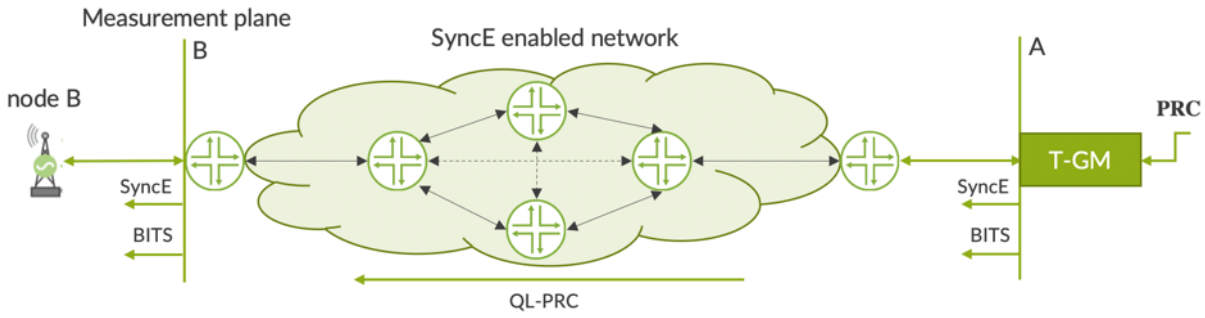


Figure 6.39 G.8261 EEC Opt.1 Wander Limit (MTIE)

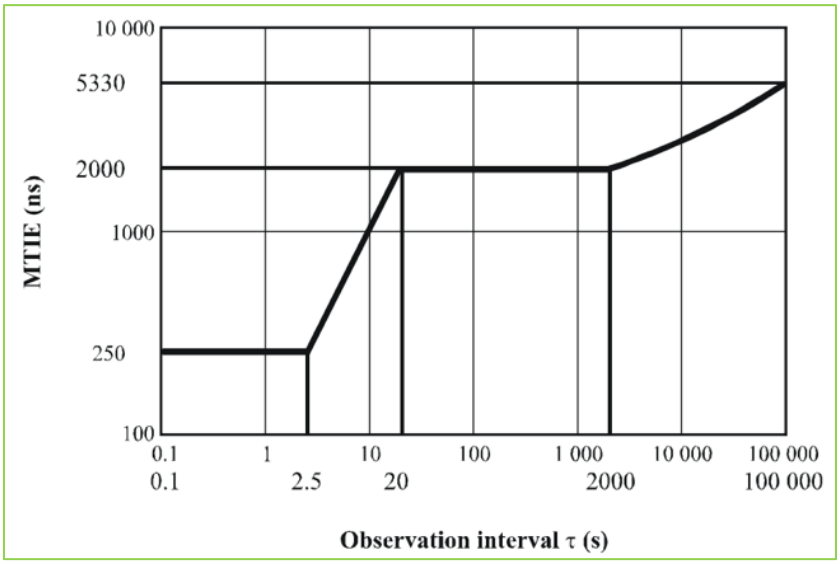


Figure 6.40 G.8261 eEEC Opt.1 Wander Limit (MTIE)

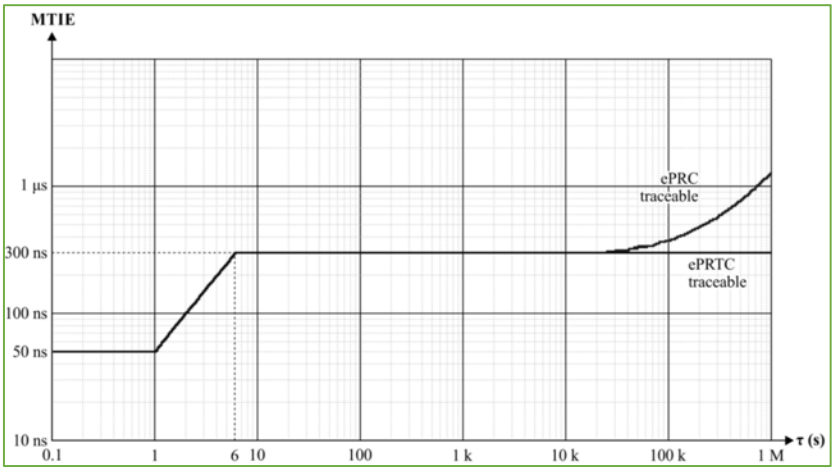


Figure 6.41 G.8261 EEC Opt.1 Wander Limit (TDEV)

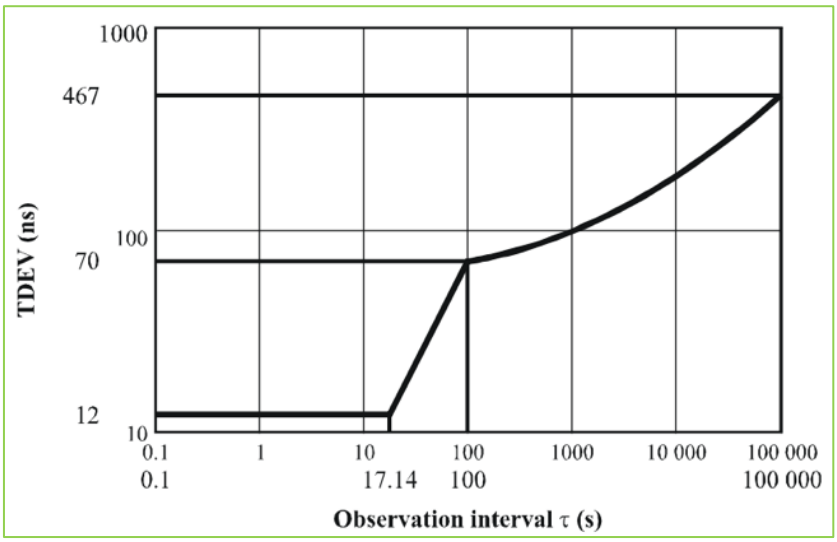


Figure 6.42 G.8261 eEEC Opt.1 Wander Limit (TDEV)

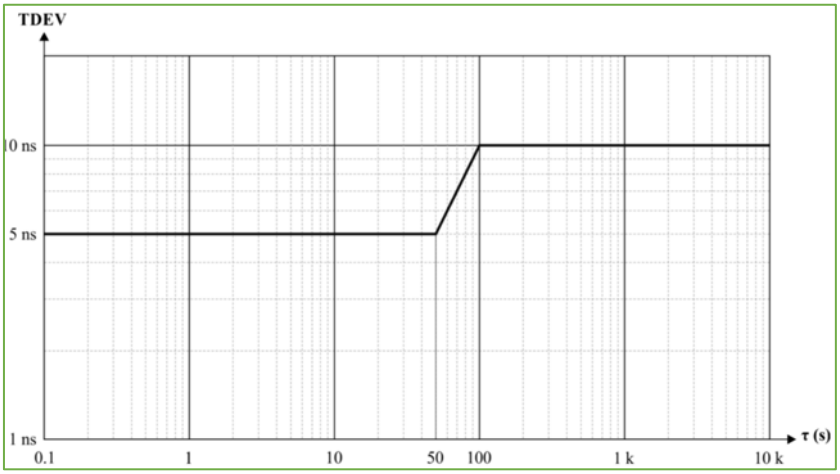
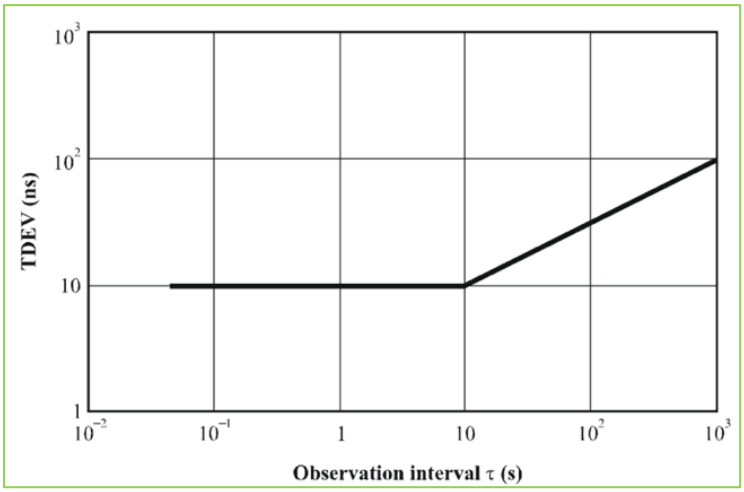


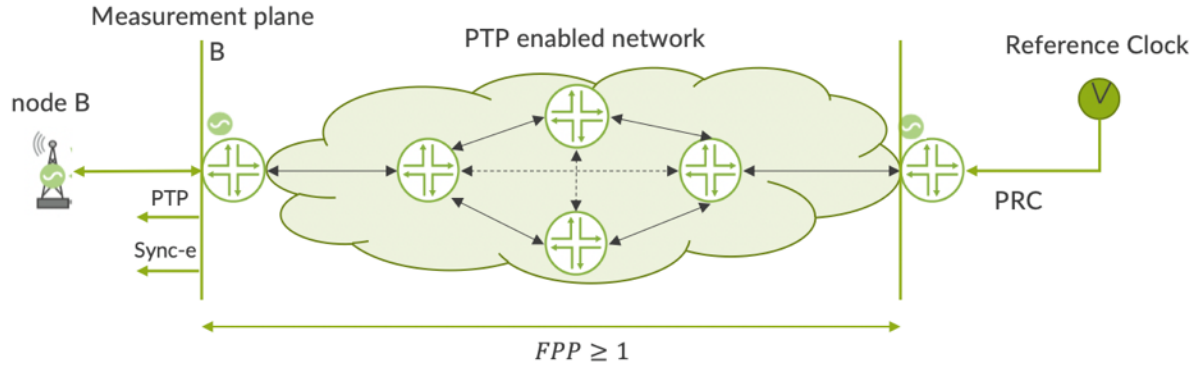
Figure 6.43 G.8261 EEC Opt.2 Wander Limit (TDEV)



G.8261.1 Network Limits

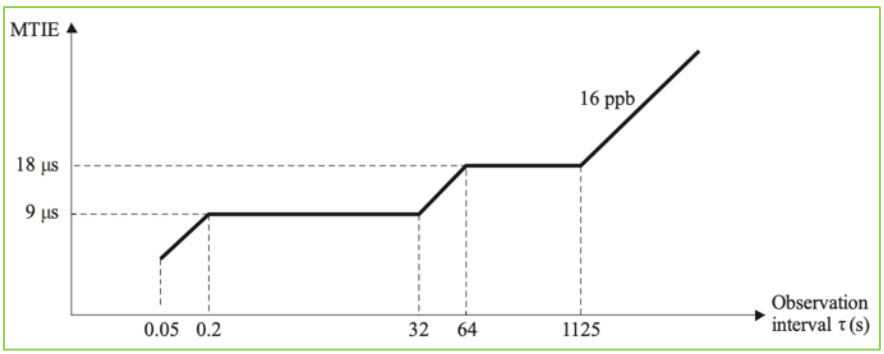
G.8261.1 defines the PDV network limits for the packet network. It describes the hypothetical reference models (HRM) for packet-based synchronization.

Figure 6.44 G.8261.1 Network Test Setup



Network Wander Limit

Figure 6.45 G.8261.1 Network Wander Limit



Network PDV Limit

As per the HRM-1 model, the packet delay variation network limit at the measurement point B is defined by ITU-T as follows.

With window interval $W = 200\ sec$ and fixed cluster range $\delta = 150\ \mu sec$ starting at the floor delay, the network transfer characteristic quantifying the proportion of delivered packets that meet the delay criterion should satisfy:

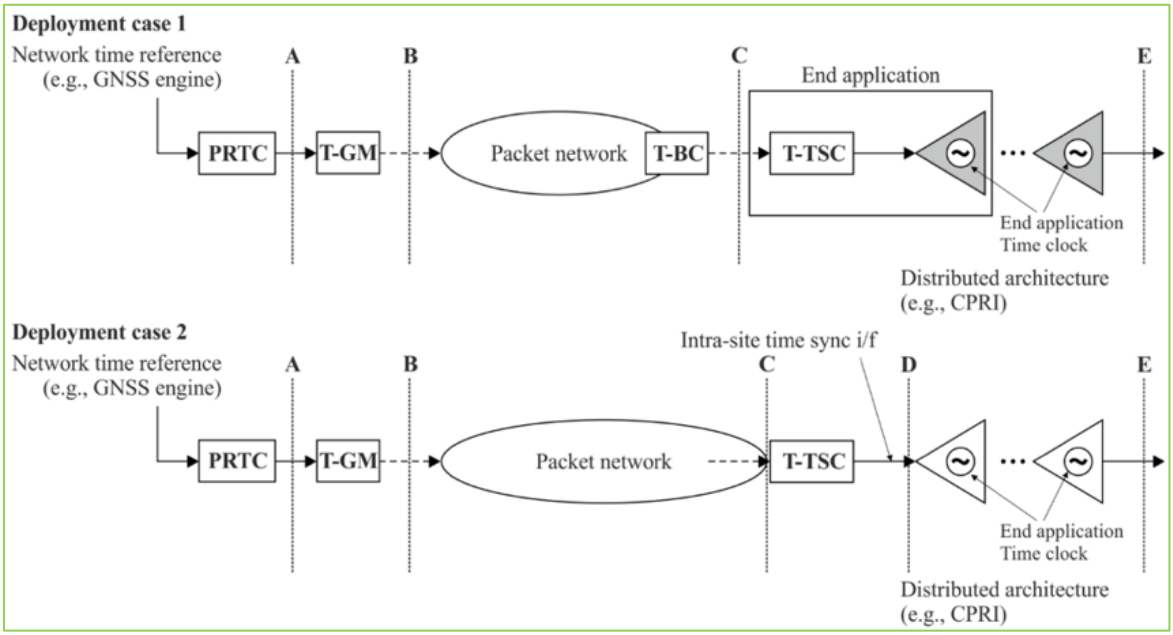
$$FPP(n, W, \delta) \geq 1\%$$

That is, the floor packet percentage must exceed 1%. This means that for any window interval of 200 sec, at least 1% of transmitted timing packets will be received within a fixed cluster, starting at the observed floor delay, and having a range of 150 µs.

G.8271.1 Network Limits

ITU-T G.8271.1 defines the network limit for packet networks with full timing support. Two network deployment models are defined in Figure 6.46.

Figure 6.46 G.8271.1 Network Deployment Model

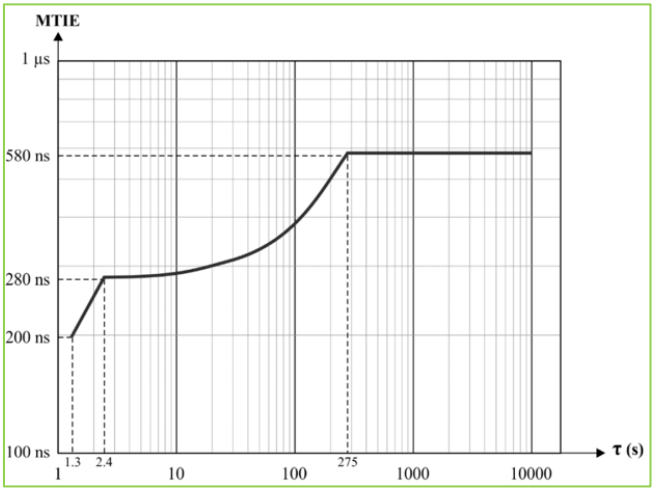


For the deployment case 1 and 2 in Figure 6.46, the network limits applicable at reference point A, i.e., at the output of the primary reference time clock (PRTC), are specified by the maximum absolute TE, max |TE| ≤ 100 ns. The same limits are applicable for a telecom grand master (T-GM) integrated into the PRTC. The network limits applicable at reference

point C for deployment case 1, and applicable at reference point D for deployment case 2, are expressed in terms of following parameters:

- Maximum absolute low pass filtered Time Error
- max $|TE_L| \leq 1100\ ns$
- Network limit for dynamic low frequency TE, $\mathrm{d}TE_L(t)$
- Peak-to-peak $\mathrm{d}TE_H(t)$ amplitude < 200 ns

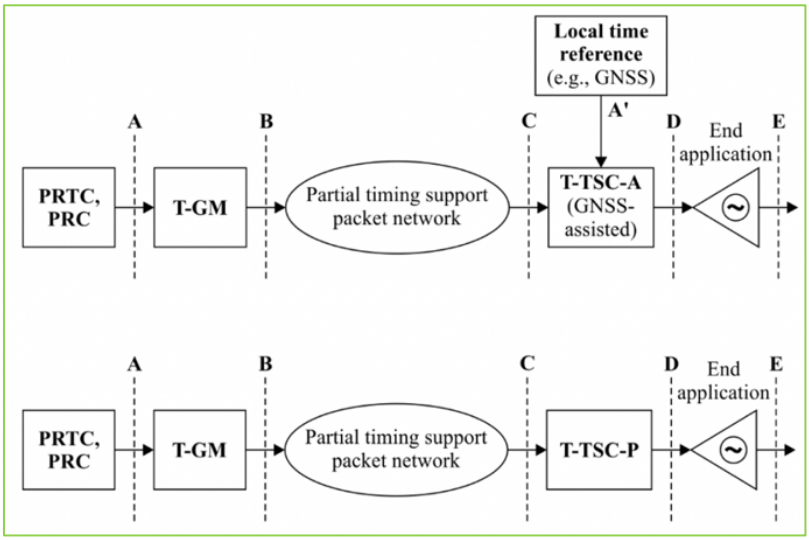
Figure 6.47 G.8271.1 Network Dynamic Low Frequency TE, Point C (MTIE)



G.8271.2 Network Limits

For the deployment case mentioned in Figure 6.48, the network limits applicable at reference point A and A', i.e., at the output of the primary reference time clock (PRTC), is specified by the maximum absolute TE, max |TE| ≤ 100 ns. A similar limit is applicable for a telecom grand master (T-GM) integrated into the PRTC.

Figure 6.48 G.8271.2 Network Deployment Model



For a network limit at reference C, two types of network limit are defined:

- Type I places less stringent requirements on the dTE generated by the network but requires a correspondingly higher performance from the clock, and;
- Type II places more stringent requirements on the dTE generated by the network with a lower performance clock.

The packet network limit value for APTS for a type I network are specified below (for type II networks, it is yet to be defined):

- Peak-to-peak pktSelected2wayTE <1100 ns
- Selection window = 200 s
- Selection percentage = 0.25%

And the packet network limit value for PTS for a type I network are specified below (for type II networks, it is yet to be defined):

- max|pktSelected2wayTE| < 1100 ns
- Selection window = 200 s
- Selection percentage = 0.25%

Summary

This chapter discussed the performance measurements for frequency and phase for individual nodes and for the network. It discussed clock specifications for various ITU-T standards G.8262/.1, G.8263, G.8273.2, G.8272, G.8273.3, G.8273.4, and network limits for G.8261, G.8261.1, G.8271.1, and G.8271.2 recommendations in detail, covering the measurement setup and pass-fail criteria and also the performance metrics.

Chapter 7

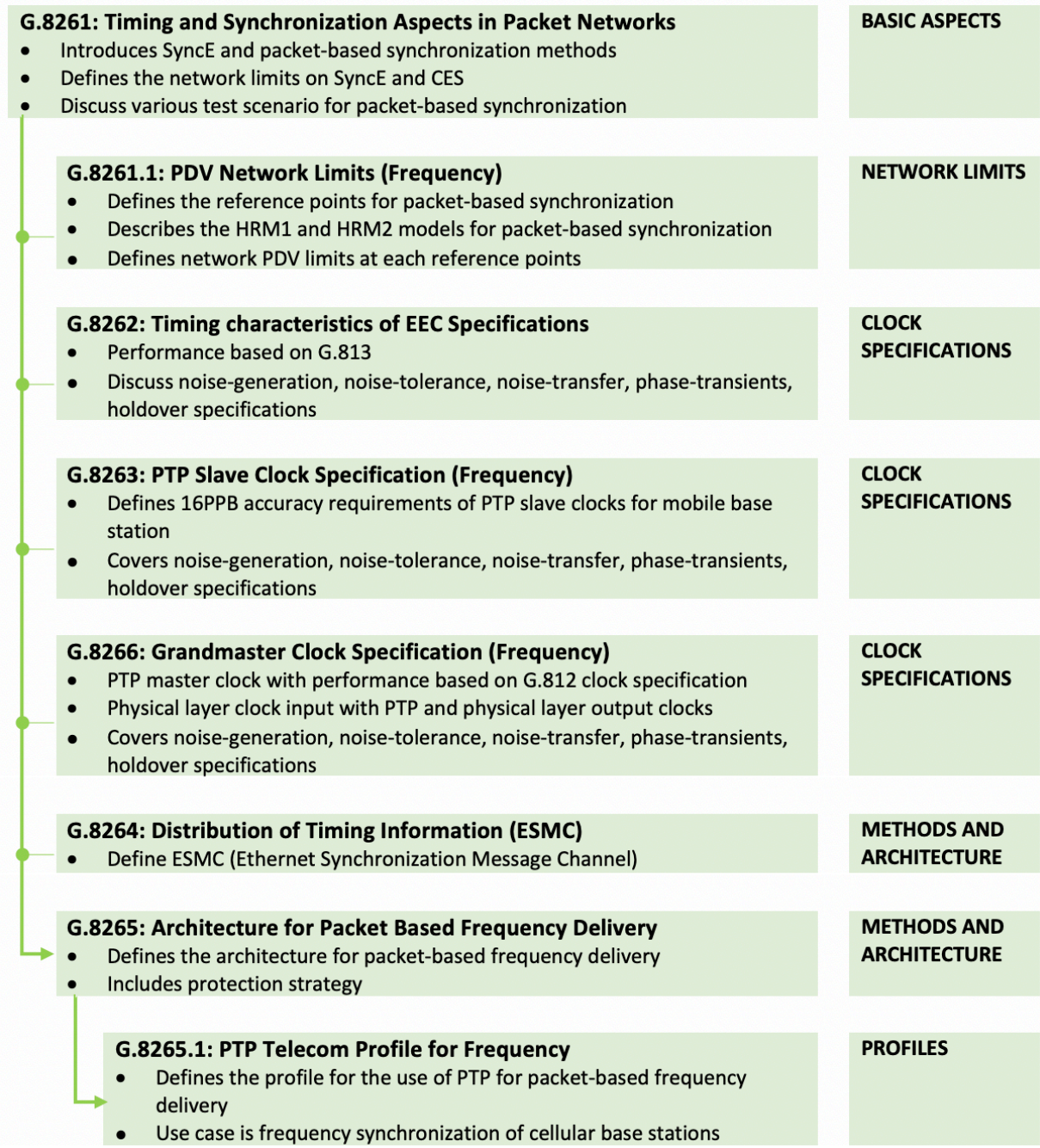
Overview of ITU-T Standardization

ITU-T recommendations are standards defining how telecommunications networks operate and interwork. For the sake of easy comprehension, let's group these recommendations into following three categories:

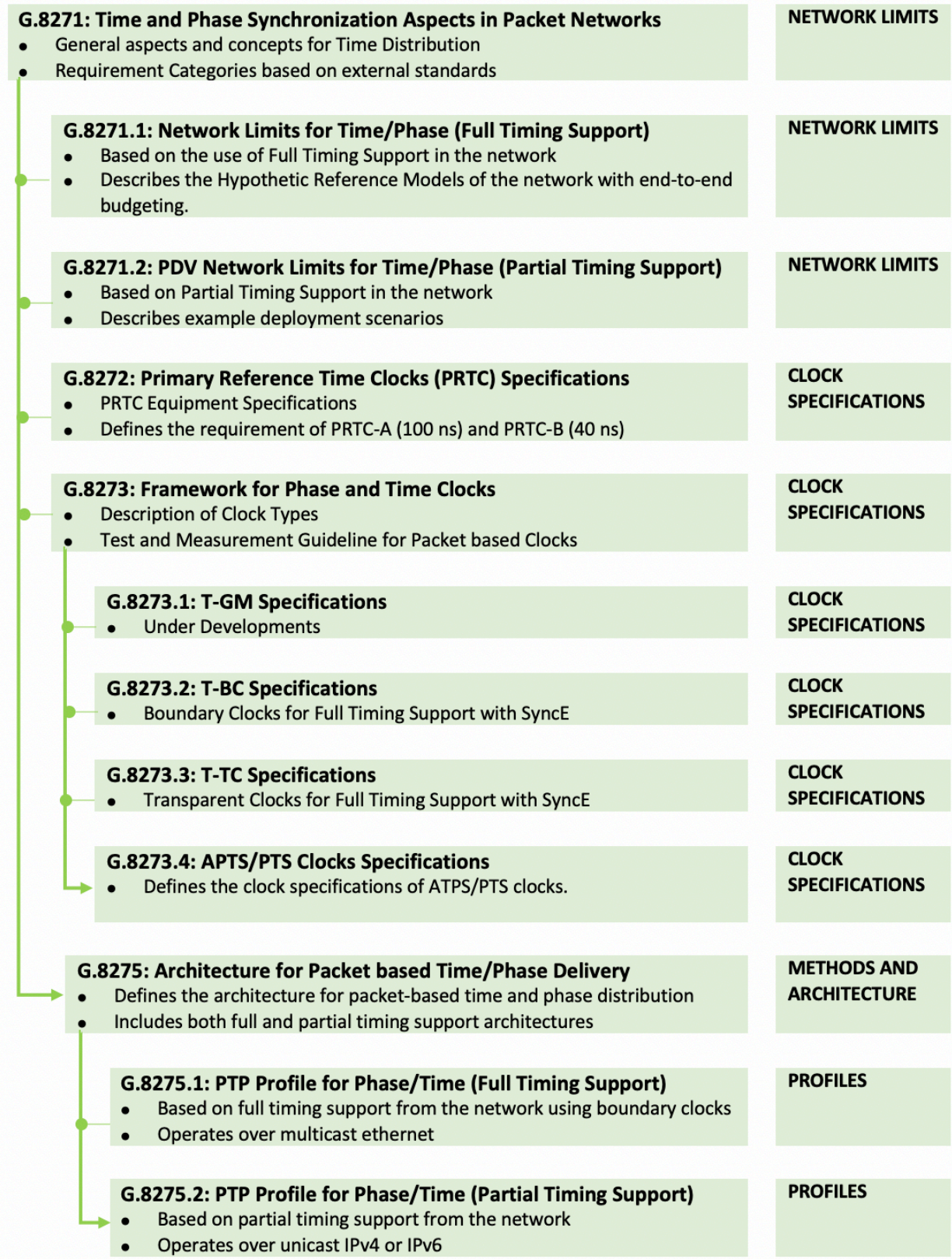
- Frequency Recommendations
- Time/Phase Recommendations
- Enhanced Time/Phase Recommendations

This chapter summarizes these three recommendations.

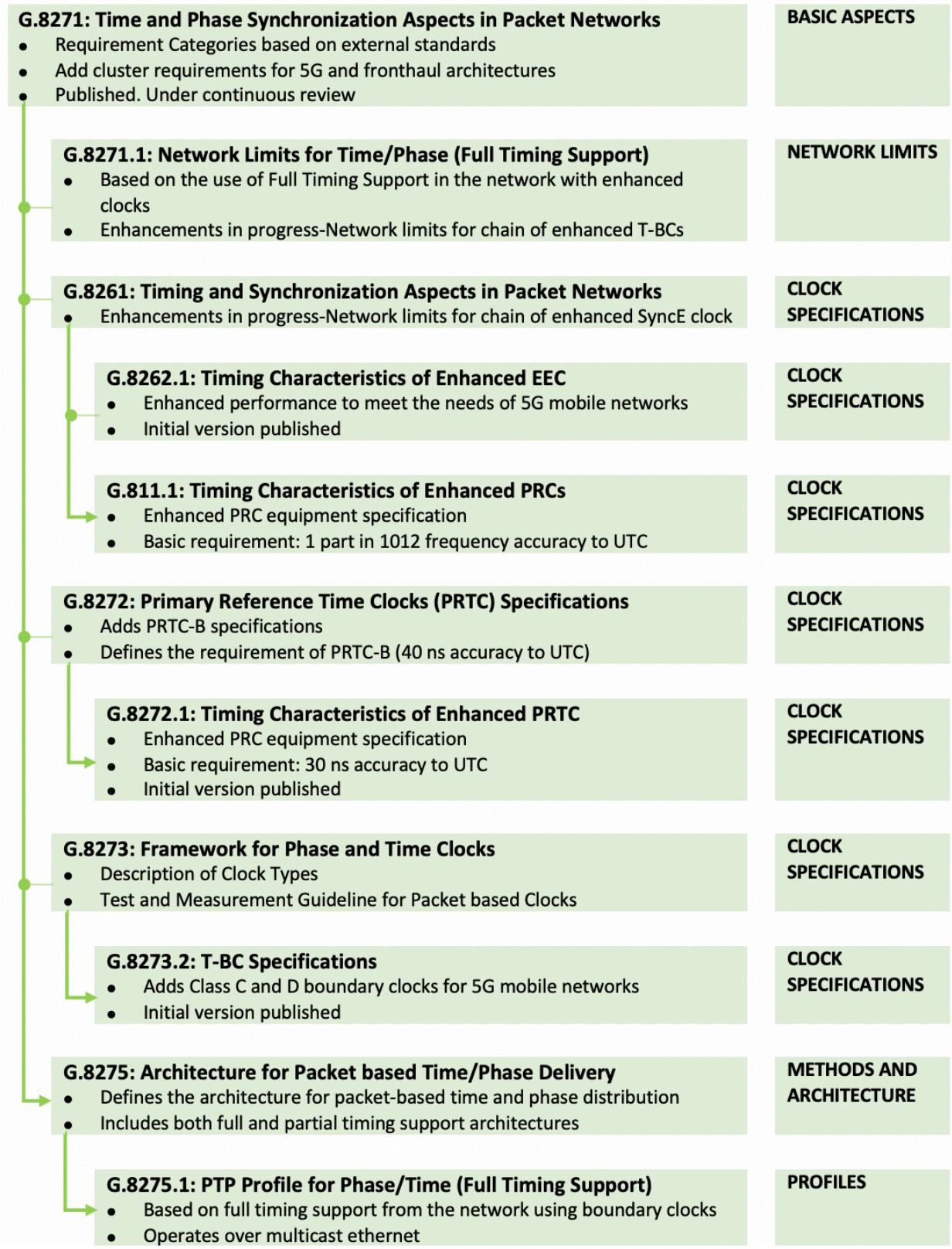
ITU-T Frequency Recommendations



ITU-T Time/Phase Recommendations



ITU-T Enhanced Time/Phase Recommendations



Appendix

Packet Decodes

PTP over IEEE 802.3 Ethernet

ANNOUNCE Packet

```
Frame 1: 82 bytes on wire (656 bits)
        Encapsulation type: Ethernet (1)
        Arrival Time: Jul 26, 2020 08:36:58.000000000 CEST
        Time shift for this packet: 0.000000000 seconds
        Epoch Time: 1595745418.000000000 seconds
        Time delta from previous captured frame: 0.000000000 seconds
        Time delta from previous displayed frame: 0.000000000 seconds
        Time since reference or first frame: 0.000000000 seconds
        Frame Number: 1
        Frame Length: 82 bytes (656 bits)
        Capture Length: 82 bytes (656 bits)
        Frame is marked: False
        Frame is ignored: False
        Protocols in frame: eth:ethertype:ptp
Ethernet II
        Destination: IEEEI&MS_00:00:00 (01:1b:19:00:00:00)
        Address: IEEEI&MS_00:00:00 (01:1b:19:00:00:00)
        .... ..0. .... .... .... .... = LG bit: Globally unique address (factory default)
        .... ...1 .... .... .... .... = IG bit: Group address (multicast/broadcast)
        Source: a0:00:00:00:00:01 (a0:00:00:00:00:01)
        Address: a0:00:00:00:00:01 (a0:00:00:00:00:01)
        .... ..0. .... .... .... .... = LG bit: Globally unique address (factory default)
        .... ...0 .... .... .... .... = IG bit: Individual address (unicast)
        Type: PTPv2 over Ethernet (IEEE1588) (0x88f7)
        Frame check sequence: 0x3e0e3d63
        FCS Status: Unverified
Precision Time Protocol (IEEE1588)
        0000 .... = transportSpecific: 0x0
        ...0 .... = 802.1as conform: False
        .... 1011 = messageId: Announce Message (0xb)
        0000 .... = Reserved: 0
        .... 0010 = versionPTP: 2
        messageLength: 64
        subdomainNumber: 24
        Reserved: 0
        flags: 0x003c
        0... .... .... .... = PTP_SECURITY: False
        .0.. .... .... .... = PTP profile Specific 2: False
        ..0. .... .... .... = PTP profile Specific 1: False
        .... .0.. .... .... = PTP_UNICAST: False
        .... ..0. .... .... = PTP_TWO_STEP: False
        .... ...0 .... .... = PTP_ALTERNATE_MASTER: False
        .... .... ..1. .... = FREQUENCY_TRACEABLE: True
        .... .... ...1 .... = TIME_TRACEABLE: True
        .... .... .... 1... = PTP_TIMESCALE: True
        .... .... .... .1.. = PTP_UTC_REASONABLE: True
        .... .... .... ..0. = PTP_LI_59: False
        .... .... .... ...0 = PTP_LI_61: False
        correction: 0.000000 nanoseconds
        correction: Ns: 0 nanoseconds
        correctionSubNs: 0 nanoseconds
        Reserved: 0
```

```
        ClockIdentity: 0x0000000000000001
        SourcePortID: 1
        sequenceId: 31752
        control: Other Message (5)
        logMessagePeriod: -3
        originTimestamp (seconds): 0
        originTimestamp (nanoseconds): 0
        originCurrentUTCOffset: 37
        priority1: 128
        grandmasterClockClass: 6
        grandmasterClockAccuracy: The time is accurate to within 100 ns (0x21)
        grandmasterClockVariance: 65535
        priority2: 128
        grandmasterClockIdentity: 0x0000000000000001
        localStepsRemoved: 0
        TimeSource: INTERNAL_OSCILLATOR (0xa0)
```

SYNC Packet

```
Frame 1: 64 bytes on wire (512 bits)
        Encapsulation type: Ethernet (1)
        Arrival Time: Jul 26, 2020 08:24:15.000000000 CEST
        Time shift for this packet: 0.000000000 seconds
        Epoch Time: 1595744655.000000000 seconds
        Time delta from previous captured frame: 0.000000000 seconds
        Time delta from previous displayed frame: 0.000000000 seconds
        Time since reference or first frame: 0.000000000 seconds
        Frame Number: 1
        Frame Length: 64 bytes (512 bits)
        Capture Length: 64 bytes (512 bits)
        Frame is marked: False
        Frame is ignored: False
        Protocols in frame: eth:ethertype:ptp
Ethernet II
        Destination: IEEEI&MS_00:00:00 (01:1b:19:00:00:00)
        Address: IEEEI&MS_00:00:00 (01:1b:19:00:00:00)
        .... ..0. .... .... .... .... = LG bit: Globally unique address (factory default)
        .... ...1 .... .... .... .... = IG bit: Group address (multicast/broadcast)
        Source: a0:00:00:00:00:01 (a0:00:00:00:00:01)
        Address: a0:00:00:00:00:01 (a0:00:00:00:00:01)
        .... ..0. .... .... .... .... = LG bit: Globally unique address (factory default)
        .... ...0 .... .... .... .... = IG bit: Individual address (unicast)
        Type: PTPv2 over Ethernet (IEEE1588) (0x88f7)
        Padding: 0000
        Frame check sequence: 0x1b0c6828
        FCS Status: Unverified
Precision Time Protocol (IEEE1588)
        0000 .... = transportSpecific: 0x0
        ...0 .... = 802.1as conform: False
        .... 0000 = messageId: Sync Message (0x0)
        0000 .... = Reserved: 0
        .... 0010 = versionPTP: 2
        messageLength: 44
        subdomainNumber: 24
        Reserved: 0
        flags: 0x0000
        0... .... .... .... = PTP_SECURITY: False
        .0.. .... .... .... = PTP profile Specific 2: False
        ..0. .... .... .... = PTP profile Specific 1: False
        .... .0.. .... .... = PTP_UNICAST: False
        .... ..0. .... .... = PTP_TWO_STEP: False
        .... ...0 .... .... = PTP_ALTERNATE_MASTER: False
        .... .... ..0. .... = FREQUENCY_TRACEABLE: False
        .... .... ...0 .... = TIME_TRACEABLE: False
        .... .... .... 0... = PTP_TIMESCALE: False
        .... .... .... .0.. = PTP_UTC_REASONABLE: False
        .... .... .... ..0. = PTP_LI_59: False
        .... .... .... ...0 = PTP_LI_61: False
        correction: 0.000000 nanoseconds
```

```
        correction: Ns: 0 nanoseconds
        correctionSubNs: 0 nanoseconds
        Reserved: 0
        ClockIdentity: 0x0000000000000001
        SourcePortID: 1
        sequenceId: 25143
        control: Sync Message (0)
        logMessagePeriod: -4
        originTimestamp (seconds): 1595742975
        originTimestamp (nanoseconds): 931739875
```

DELAY-REQUEST Packet

```
Frame 1: 64 bytes on wire (512 bits)
        Encapsulation type: Ethernet (1)
        Arrival Time: Jul 26, 2020 08:29:19.000000000 CEST
        Time shift for this packet: 0.000000000 seconds
        Epoch Time: 1595744959.000000000 seconds
        Time delta from previous captured frame: 0.000000000 seconds
        Time delta from previous displayed frame: 0.000000000 seconds
        Time since reference or first frame: 0.000000000 seconds
        Frame Number: 1
        Frame Length: 64 bytes (512 bits)
        Capture Length: 64 bytes (512 bits)
        Frame is marked: False
        Frame is ignored: False
        Protocols in frame: eth:ethertype:ptp
Ethernet II
        Destination: IEEEI&MS_00:00:00 (01:1b:19:00:00:00)
        Address: IEEEI&MS_00:00:00 (01:1b:19:00:00:00)
        .... ..0. .... .... .... .... = LG bit: Globally unique address (factory default)
        .... ...1 .... .... .... .... = IG bit: Group address (multicast/broadcast)
        Source: Ericsson_7d:d6:8f (98:a4:04:7d:d6:8f)
        Address: Ericsson_7d:d6:8f (98:a4:04:7d:d6:8f)
        .... ..0. .... .... .... .... = LG bit: Globally unique address (factory default)
        .... ...0 .... .... .... .... = IG bit: Individual address (unicast)
        Type: PTPv2 over Ethernet (IEEE1588) (0x88f7)
        Padding: 0000
        Frame check sequence: 0xa465d16c
        FCS Status: Unverified
Precision Time Protocol (IEEE1588)
        0000 .... = transportSpecific: 0x0
        ...0 .... = 802.1as conform: False
        .... 0001 = messageId: Delay_Req Message (0x1)
        0000 .... = Reserved: 0
        .... 0010 = versionPTP: 2
        messageLength: 44
        subdomainNumber: 24
        Reserved: 0
        flags: 0x0000
        0... .... .... .... = PTP_SECURITY: False
        .0.. .... .... .... = PTP profile Specific 2: False
        ..0. .... .... .... = PTP profile Specific 1: False
        .... .0.. .... .... = PTP_UNICAST: False
        .... ..0. .... .... = PTP_TWO_STEP: False
        .... ...0 .... .... = PTP_ALTERNATE_MASTER: False
        .... .... ..0. .... = FREQUENCY_TRACEABLE: False
        .... .... ...0 .... = TIME_TRACEABLE: False
        .... .... .... 0... = PTP_TIMESCALE: False
        .... .... .... .0.. = PTP_UTC_REASONABLE: False
        .... .... .... ..0. = PTP_LI_59: False
        .... .... .... ...0 = PTP_LI_61: False
        correction: 224216593.000000 nanoseconds
        correction: Ns: 224216593 nanoseconds
        correctionSubNs: 0 nanoseconds
        Reserved: 0
        ClockIdentity: 0x98a404fffe7dd6ff
        MAC Vendor: Ericsson
        SourcePortID: 1
```

```
        sequenceId: 5402
        control: Delay_Req Message (1)
        logMessagePeriod: 127
        originTimestamp (seconds): 0
        originTimestamp (nanoseconds): 0
```

DELAY-RESPONSE Packet

```
Frame 1: 72 bytes on wire (576 bits)
        Encapsulation type: Ethernet (1)
        Arrival Time: Jul 26, 2020 08:33:54.000000000 CEST
        Time shift for this packet: 0.000000000 seconds
        Epoch Time: 1595745234.000000000 seconds
        Time delta from previous captured frame: 0.000000000 seconds
        Time delta from previous displayed frame: 0.000000000 seconds
        Time since reference or first frame: 0.000000000 seconds
        Frame Number: 1
        Frame Length: 72 bytes (576 bits)
        Capture Length: 72 bytes (576 bits)
        Frame is marked: False
        Frame is ignored: False
        Protocols in frame: eth:ethertype:ptp
Ethernet II
        Destination: IEEEI&MS_00:00:00 (01:1b:19:00:00:00)
        Address: IEEEI&MS_00:00:00 (01:1b:19:00:00:00)
        .... ..0. .... .... .... .... = LG bit: Globally unique address (factory default)
        .... ...1 .... .... .... .... = IG bit: Group address (multicast/broadcast)
        Source: a0:00:00:00:00:01 (a0:00:00:00:00:01)
        Address: a0:00:00:00:00:01 (a0:00:00:00:00:01)
        .... ..0. .... .... .... .... = LG bit: Globally unique address (factory default)
        .... ...0 .... .... .... .... = IG bit: Individual address (unicast)
        Type: PTPv2 over Ethernet (IEEE1588) (0x88f7)
        Frame check sequence: 0x9ea953b7
        FCS Status: Unverified
Precision Time Protocol (IEEE1588)
        0000 .... = transportSpecific: 0x0
        ...0 .... = 802.1as conform: False
        .... 1001 = messageId: Delay_Resp Message (0x9)
        0000 .... = Reserved: 0
        .... 0010 = versionPTP: 2
        messageLength: 54
        subdomainNumber: 24
        Reserved: 0
        flags: 0x0000
        0... .... .... .... = PTP_SECURITY: False
        .0.. .... .... .... = PTP profile Specific 2: False
        ..0. .... .... .... = PTP profile Specific 1: False
        .... .0.. .... .... = PTP_UNICAST: False
        .... ..0. .... .... = PTP_TWO_STEP: False
        .... ...0 .... .... = PTP_ALTERNATE_MASTER: False
        .... .... ..0. .... = FREQUENCY_TRACEABLE: False
        .... .... ...0 .... = TIME_TRACEABLE: False
        .... .... .... 0... = PTP_TIMESCALE: False
        .... .... .... .0.. = PTP_UTC_REASONABLE: False
        .... .... .... ..0. = PTP_LI_59: False
        .... .... .... ...0 = PTP_LI_61: False
        correction: 292425169.000000 nanoseconds
        correction: Ns: 292425169 nanoseconds
        correctionSubNs: 0 nanoseconds
        Reserved: 0
        ClockIdentity: 0x0000000000000001
        SourcePortID: 1
        sequenceId: 5403
        control: Delay_Resp Message (3)
        logMessagePeriod: -4
        receiveTimestamp (seconds): 1595742976
        receiveTimestamp (nanoseconds): 129499775
        requestingSourcePortIdentity: 0x98a404fffe7dd6ff
        requestingSourcePortId: 1
```

PTP over UDP over IPv4

Signalling Request for ANNOUNCE Packet

```
Frame 1: 100 bytes on wire (800 bits)
        Encapsulation type: Ethernet (1)
        Arrival Time: Jul 26, 2020 10:58:33.000000000 CEST
        Time shift for this packet: 0.000000000 seconds
        Epoch Time: 1595753913.000000000 seconds
        Time delta from previous captured frame: 0.000000000 seconds
        Time delta from previous displayed frame: 0.000000000 seconds
        Time since reference or first frame: 0.000000000 seconds
        Frame Number: 1
        Frame Length: 100 bytes (800 bits)
        Capture Length: 100 bytes (800 bits)
        Frame is marked: False
        Frame is ignored: False
        Protocols in frame: eth:ethertype:ip:udp:ptp
Ethernet II
        Destination: a0:00:00:00:00:01 (a0:00:00:00:00:01)
        Address: a0:00:00:00:00:01 (a0:00:00:00:00:01)
        .... ..0. .... .... .... .... = LG bit: Globally unique address (factory default)
        .... ...0 .... .... .... .... = IG bit: Individual address (unicast)
        Source: JuniperN_e2:d0:32 (08:b2:58:e2:d0:32)
        Address: JuniperN_e2:d0:32 (08:b2:58:e2:d0:32)
        .... ..0. .... .... .... .... = LG bit: Globally unique address (factory default)
        .... ...0 .... .... .... .... = IG bit: Individual address (unicast)
        Type: IPv4 (0x0800)
        Frame check sequence: 0x9815d38a
        FCS Status: Unverified
Internet Protocol Version 4
        0100 .... = Version: 4
        .... 0101 = Header Length: 20 bytes (5)
        Differentiated Services Field: 0xe0 (DSCP: CS7, ECN: Not-ECT)
        1110 00.. = Differentiated Services Codepoint: Class Selector 7 (56)
        .... ..00 = Explicit Congestion Notification: Not ECN-Capable Transport (0)
        Total Length: 82
        Identification: 0x0000 (0)
        Flags: 0x4000, Don't fragment
        0... .... .... .... = Reserved bit: Not set
        .1.. .... .... .... = Don't fragment: Set
        ..0. .... .... .... = More fragments: Not set
        Fragment offset: 0
        Time to live: 63
        Protocol: UDP (17)
        Header checksum: 0x26b9
        Header checksum status: Unverified
        Source: 10.0.0.2
        Destination: 10.0.0.1
User Datagram Protocol
        Source Port: 320
        Destination Port: 320
        Length: 62
        Checksum: 0xe943
        Checksum Status: Unverified
        Stream index: 0
        Timestamps
        Time since first frame: 0.000000000 seconds
        Time since previous frame: 0.000000000 seconds
Precision Time Protocol (IEEE1588)
        0000 .... = transportSpecific: 0x0
        ...0 .... = V1 Compatibility: False
        .... 1100 = messageId: Signalling Message (0xc)
        0000 .... = Reserved: 0
        .... 0010 = versionPTP: 2
        messageLength: 54
        subdomainNumber: 0
        Reserved: 0
```

```
        flags: 0x0400
        0... .... .... .... = PTP_SECURITY: False
        .0.. .... .... .... = PTP profile Specific 2: False
        ..0. .... .... .... = PTP profile Specific 1: False
        .... .1.. .... .... = PTP_UNICAST: True
        .... ..0. .... .... = PTP_TWO_STEP: False
        .... ...0 .... .... = PTP_ALTERNATE_MASTER: False
        .... .... ..0. .... = FREQUENCY_TRACEABLE: False
        .... .... ...0 .... = TIME_TRACEABLE: False
        .... .... .... 0... = PTP_TIMESCALE: False
        .... .... .... .0.. = PTP_UTC_REASONABLE: False
        .... .... .... ..0. = PTP_LI_59: False
        .... .... .... ...0 = PTP_LI_61: False
        correction: 0.000000 nanoseconds
        correction: Ns: 0 nanoseconds
        correctionSubNs: 0 nanoseconds
        Reserved: 0
        ClockIdentity: 0x08b258fffee2d7d0
        MAC Vendor: JuniperN
        SourcePortID: 1
        sequenceId: 87
        control: Other Message (5)
        logMessagePeriod: 127
        targetPortIdentity: 0xffffffffffffffff
        targetPortId: 65535
        tlvType: Request unicast transmission (4)
        lengthField: 6
        1011 .... = messageType: Announce Message (0xb)
        logInterMessagePeriod: 1
        period: every 2 seconds
        rate: 0.5 packets/sec
        durationField: 300 seconds
```

Signalling Grant for ANNOUNCE Packet

```
Frame 1: 102 bytes on wire (816 bits)
        Encapsulation type: Ethernet (1)
        Arrival Time: Jul 26, 2020 10:59:54.000000000 CEST
        Time shift for this packet: 0.000000000 seconds
        Epoch Time: 1595753994.000000000 seconds
        Time delta from previous captured frame: 0.000000000 seconds
        Time delta from previous displayed frame: 0.000000000 seconds
        Time since reference or first frame: 0.000000000 seconds
        Frame Number: 1
        Frame Length: 102 bytes (816 bits)
        Capture Length: 102 bytes (816 bits)
        Frame is marked: False
        Frame is ignored: False
        Protocols in frame: eth:ethertype:ip:udp:ptp
Ethernet II
        Destination: JuniperN_e2:d0:32 (08:b2:58:e2:d0:32)
        Address: JuniperN_e2:d0:32 (08:b2:58:e2:d0:32)
        .... ..0. .... .... .... .... = LG bit: Globally unique address (factory default)
        .... ...0 .... .... .... .... = IG bit: Individual address (unicast)
        Source: a0:00:00:00:00:01 (a0:00:00:00:00:01)
        Address: a0:00:00:00:00:01 (a0:00:00:00:00:01)
        .... ..0. .... .... .... .... = LG bit: Globally unique address (factory default)
        .... ...0 .... .... .... .... = IG bit: Individual address (unicast)
        Type: IPv4 (0x0800)
        Frame check sequence: 0x9ac75bdd
        FCS Status: Unverified
Internet Protocol Version 4
        0100 .... = Version: 4
        .... 0101 = Header Length: 20 bytes (5)
        Differentiated Services Field: 0xb8 (DSCP: EF PHB, ECN: Not-ECT)
        1011 10.. = Differentiated Services Codepoint: Expedited Forwarding (46)
        .... ..00 = Explicit Congestion Notification: Not ECN-Capable Transport (0)
        Total Length: 84
        Identification: 0x0000 (0)
```

```
        Flags: 0x4000, Don't fragment
        0... .... .... .... = Reserved bit: Not set
        .1.. .... .... .... = Don't fragment: Set
        ..0. .... .... .... = More fragments: Not set
        Fragment offset: 0
        Time to live: 64
        Protocol: UDP (17)
        Header checksum: 0x25df
        Header checksum status: Unverified
        Source: 10.0.0.1
        Destination: 10.0.0.2
User Datagram Protocol
        Source Port: 320
        Destination Port: 320
        Length: 64
        Checksum: [missing]
        Checksum Status: Not present
        Stream index: 0
        Timestamps
        Time since first frame: 0.000000000 seconds
        Time since previous frame: 0.000000000 seconds
Precision Time Protocol (IEEE1588)
        0000 .... = transportSpecific: 0x0
        ...0 .... = V1 Compatibility: False
        .... 1100 = messageId: Signalling Message (0xc)
        0000 .... = Reserved: 0
        .... 0010 = versionPTP: 2
        messageLength: 56
        subdomainNumber: 0
        Reserved: 0
        flags: 0x0400
        0... .... .... .... = PTP_SECURITY: False
        .0.. .... .... .... = PTP profile Specific 2: False
        ..0. .... .... .... = PTP profile Specific 1: False
        .... .1.. .... .... = PTP_UNICAST: True
        .... ..0. .... .... = PTP_TWO_STEP: False
        .... ...0 .... .... = PTP_ALTERNATE_MASTER: False
        .... .... ..0. .... = FREQUENCY_TRACEABLE: False
        .... .... ...0 .... = TIME_TRACEABLE: False
        .... .... .... 0... = PTP_TIMESCALE: False
        .... .... .... .0.. = PTP_UTC_REASONABLE: False
        .... .... .... ..0. = PTP_LI_59: False
        .... .... .... ...0 = PTP_LI_61: False
        correction: 0.000000 nanoseconds
        correction: Ns: 0 nanoseconds
        correctionSubNs: 0 nanoseconds
        Reserved: 0
        ClockIdentity: 0x0000000000000001
        SourcePortID: 1
        sequenceId: 87
        control: Other Message (5)
        logMessagePeriod: 127
        targetPortIdentity: 0x08b258fffee2d7d0
        targetPortId: 1
        tlvType: Grant unicast transmission (5)
        lengthField: 8
        1011 .... = messageType: Announce Message (0xb)
        logInterMessagePeriod: 1
        period: every 2 seconds
        rate: 0.5 packets/sec
        durationField: 300 seconds
        .... ...1 = renewalInvited: True
```

Signalling Request for SYNC Packet

```
Frame 1: 100 bytes on wire (800 bits)
        Encapsulation type: Ethernet (1)
        Arrival Time: Jul 26, 2020 11:01:30.000000000 CEST
        Time shift for this packet: 0.000000000 seconds
```

```
        Epoch Time: 1595754090.000000000 seconds
        Time delta from previous captured frame: 0.000000000 seconds
        Time delta from previous displayed frame: 0.000000000 seconds
        Time since reference or first frame: 0.000000000 seconds
        Frame Number: 1
        Frame Length: 100 bytes (800 bits)
        Capture Length: 100 bytes (800 bits)
        Frame is marked: False
        Frame is ignored: False
        Protocols in frame: eth:ethertype:ip:udp:ptp
Ethernet II
        Destination: a0:00:00:00:00:01 (a0:00:00:00:00:01)
        Address: a0:00:00:00:00:01 (a0:00:00:00:00:01)
        .... ..0. .... .... .... .... = LG bit: Globally unique address (factory default)
        .... ...0 .... .... .... .... = IG bit: Individual address (unicast)
        Source: JuniperN_e2:d0:32 (08:b2:58:e2:d0:32)
        Address: JuniperN_e2:d0:32 (08:b2:58:e2:d0:32)
        .... ..0. .... .... .... .... = LG bit: Globally unique address (factory default)
        .... ...0 .... .... .... .... = IG bit: Individual address (unicast)
        Type: IPv4 (0x0800)
        Frame check sequence: 0xb823e723
        FCS Status: Unverified
Internet Protocol Version 4
        0100 .... = Version: 4
        .... 0101 = Header Length: 20 bytes (5)
        Differentiated Services Field: 0xe0 (DSCP: CS7, ECN: Not-ECT)
        1110 00.. = Differentiated Services Codepoint: Class Selector 7 (56)
        .... ..00 = Explicit Congestion Notification: Not ECN-Capable Transport (0)
        Total Length: 82
        Identification: 0x0000 (0)
        Flags: 0x4000, Don't fragment
        0... .... .... .... = Reserved bit: Not set
        .1.. .... .... .... = Don't fragment: Set
        ..0. .... .... .... = More fragments: Not set
        Fragment offset: 0
        Time to live: 63
        Protocol: UDP (17)
        Header checksum: 0x26b9
        Header checksum status: Unverified
        Source: 10.0.0.2
        Destination: 10.0.0.1
User Datagram Protocol
        Source Port: 320
        Destination Port: 320
        Length: 62
        Checksum: 0x984a
        Checksum Status: Unverified
        Stream index: 0
        Timestamps
        Time since first frame: 0.000000000 seconds
        Time since previous frame: 0.000000000 seconds
Precision Time Protocol (IEEE1588)
        0000 .... = transportSpecific: 0x0
        ...0 .... = V1 Compatibility: False
        .... 1100 = messageId: Signalling Message (0xc)
        0000 .... = Reserved: 0
        .... 0010 = versionPTP: 2
        messageLength: 54
        subdomainNumber: 0
        Reserved: 0
        flags: 0x0400
        0... .... .... .... = PTP_SECURITY: False
        .0.. .... .... .... = PTP profile Specific 2: False
        ..0. .... .... .... = PTP profile Specific 1: False
        .... .1.. .... .... = PTP_UNICAST: True
        .... ..0. .... .... = PTP_TWO_STEP: False
        .... ...0 .... .... = PTP_ALTERNATE_MASTER: False
        .... .... ..0. .... = FREQUENCY_TRACEABLE: False
        .... .... ...0 .... = TIME_TRACEABLE: False
```

```
        .... .... .... 0... = PTP_TIMESCALE: False
        .... .... .... .0.. = PTP_UTC_REASONABLE: False
        .... .... .... ..0. = PTP_LI_59: False
        .... .... .... ...0 = PTP_LI_61: False
        correction: 0.000000 nanoseconds
        correction: Ns: 0 nanoseconds
        correctionSubNs: 0 nanoseconds
        Reserved: 0
        ClockIdentity: 0x08b258fffee2d7d0
        MAC Vendor: JuniperN
        SourcePortID: 1
        sequenceId: 88
        control: Other Message (5)
        logMessagePeriod: 127
        targetPortIdentity: 0xffffffffffffffff
        targetPortId: 65535
        tlvType: Request unicast transmission (4)
        lengthField: 6
        0000 .... = messageType: Sync Message (0x0)
        logInterMessagePeriod: -6
        period: every 0.015625 seconds
        rate: 64 packets/sec
        durationField: 300 seconds
```

Signalling Grant for SYNC Packet

```
Frame 1: 102 bytes on wire (816 bits)
        Encapsulation type: Ethernet (1)
        Arrival Time: Jul 26, 2020 11:03:10.000000000 CEST
        Time shift for this packet: 0.000000000 seconds
        Epoch Time: 1595754190.000000000 seconds
        Time delta from previous captured frame: 0.000000000 seconds
        Time delta from previous displayed frame: 0.000000000 seconds
        Time since reference or first frame: 0.000000000 seconds
        Frame Number: 1
        Frame Length: 102 bytes (816 bits)
        Capture Length: 102 bytes (816 bits)
        Frame is marked: False
        Frame is ignored: False
        Protocols in frame: eth:ethertype:ip:udp:ptp
Ethernet II
        Destination: JuniperN_e2:d0:32 (08:b2:58:e2:d0:32)
        Address: JuniperN_e2:d0:32 (08:b2:58:e2:d0:32)
        .... ..0. .... .... .... .... = LG bit: Globally unique address (factory default)
        .... ...0 .... .... .... .... = IG bit: Individual address (unicast)
        Source: a0:00:00:00:00:01 (a0:00:00:00:00:01)
        Address: a0:00:00:00:00:01 (a0:00:00:00:00:01)
        .... ..0. .... .... .... .... = LG bit: Globally unique address (factory default)
        .... ...0 .... .... .... .... = IG bit: Individual address (unicast)
        Type: IPv4 (0x0800)
        Frame check sequence: 0x01108f8f
        FCS Status: Unverified
Internet Protocol Version 4
        0100 .... = Version: 4
        .... 0101 = Header Length: 20 bytes (5)
        Differentiated Services Field: 0xb8 (DSCP: EF PHB, ECN: Not-ECT)
        1011 10.. = Differentiated Services Codepoint: Expedited Forwarding (46)
        .... ..00 = Explicit Congestion Notification: Not ECN-Capable Transport (0)
        Total Length: 84
        Identification: 0x0000 (0)
        Flags: 0x4000, Don't fragment
        0... .... .... .... = Reserved bit: Not set
        .1.. .... .... .... = Don't fragment: Set
        ..0. .... .... .... = More fragments: Not set
        Fragment offset: 0
        Time to live: 64
        Protocol: UDP (17)
        Header checksum: 0x25df
        Header checksum status: Unverified
```

```
        Source: 10.0.0.1
        Destination: 10.0.0.2
User Datagram Protocol
        Source Port: 320
        Destination Port: 320
        Length: 64
        Checksum: [missing]
        Checksum Status: Not present
        Stream index: 0
        Timestamps
        Time since first frame: 0.000000000 seconds
        Time since previous frame: 0.000000000 seconds
Precision Time Protocol (IEEE1588)
        0000 .... = transportSpecific: 0x0
        ...0 .... = V1 Compatibility: False
        .... 1100 = messageId: Signalling Message (0xc)
        0000 .... = Reserved: 0
        .... 0010 = versionPTP: 2
        messageLength: 56
        subdomainNumber: 0
        Reserved: 0
        flags: 0x0400
        0... .... .... .... = PTP_SECURITY: False
        .0.. .... .... .... = PTP profile Specific 2: False
        ..0. .... .... .... = PTP profile Specific 1: False
        .... .1.. .... .... = PTP_UNICAST: True
        .... ..0. .... .... = PTP_TWO_STEP: False
        .... ...0 .... .... = PTP_ALTERNATE_MASTER: False
        .... .... ..0. .... = FREQUENCY_TRACEABLE: False
        .... .... ...0 .... = TIME_TRACEABLE: False
        .... .... .... 0... = PTP_TIMESCALE: False
        .... .... .... .0.. = PTP_UTC_REASONABLE: False
        .... .... .... ..0. = PTP_LI_59: False
        .... .... .... ...0 = PTP_LI_61: False
        correction: 0.000000 nanoseconds
        correction: Ns: 0 nanoseconds
        correctionSubNs: 0 nanoseconds
        Reserved: 0
        ClockIdentity: 0x0000000000000001
        SourcePortID: 1
        sequenceId: 88
        control: Other Message (5)
        logMessagePeriod: 127
        targetPortIdentity: 0x08b258fffee2d7d0
        targetPortId: 1
        tlvType: Grant unicast transmission (5)
        lengthField: 8
        0000 .... = messageType: Sync Message (0x0)
        logInterMessagePeriod: -6
        period: every 0.015625 seconds
        rate: 64 packets/sec
        durationField: 300 seconds
        .... ...1 = renewalInvited: True
```

Signalling Request for DELAY-RESPONSE Packet

```
Frame 1: 100 bytes on wire (800 bits)
        Encapsulation type: Ethernet (1)
        Arrival Time: Jul 26, 2020 11:04:24.000000000 CEST
        Time shift for this packet: 0.000000000 seconds
        Epoch Time: 1595754264.000000000 seconds
        Time delta from previous captured frame: 0.000000000 seconds
        Time delta from previous displayed frame: 0.000000000 seconds
        Time since reference or first frame: 0.000000000 seconds
        Frame Number: 1
        Frame Length: 100 bytes (800 bits)
        Capture Length: 100 bytes (800 bits)
        Frame is marked: False
        Frame is ignored: False
```

```
        Protocols in frame: eth:ethertype:ip:udp:ptp
Ethernet II
        Destination: a0:00:00:00:00:01 (a0:00:00:00:00:01)
        Address: a0:00:00:00:00:01 (a0:00:00:00:00:01)
        .... ..0. .... .... .... .... = LG bit: Globally unique address (factory default)
        .... ...0 .... .... .... .... = IG bit: Individual address (unicast)
        Source: JuniperN_e2:d0:32 (08:b2:58:e2:d0:32)
        Address: JuniperN_e2:d0:32 (08:b2:58:e2:d0:32)
        .... ..0. .... .... .... .... = LG bit: Globally unique address (factory default)
        .... ...0 .... .... .... .... = IG bit: Individual address (unicast)
        Type: IPv4 (0x0800)
        Frame check sequence: 0xa729f258
        FCS Status: Unverified
Internet Protocol Version 4
        0100 .... = Version: 4
        .... 0101 = Header Length: 20 bytes (5)
        Differentiated Services Field: 0xe0 (DSCP: CS7, ECN: Not-ECT)
        1110 00.. = Differentiated Services Codepoint: Class Selector 7 (56)
        .... ..00 = Explicit Congestion Notification: Not ECN-Capable Transport (0)
        Total Length: 82
        Identification: 0x0000 (0)
        Flags: 0x4000, Don't fragment
        0... .... .... .... = Reserved bit: Not set
        .1.. .... .... .... = Don't fragment: Set
        ..0. .... .... .... = More fragments: Not set
        Fragment offset: 0
        Time to live: 63
        Protocol: UDP (17)
        Header checksum: 0x26b9
        Header checksum status: Unverified
        Source: 10.0.0.2
        Destination: 10.0.0.1
User Datagram Protocol
        Source Port: 320
        Destination Port: 320
        Length: 62
        Checksum: 0x0847
        Checksum Status: Unverified
        Stream index: 0
        Timestamps
        Time since first frame: 0.000000000 seconds
        Time since previous frame: 0.000000000 seconds
Precision Time Protocol (IEEE1588)
        0000 .... = transportSpecific: 0x0
        ...0 .... = V1 Compatibility: False
        .... 1100 = messageId: Signalling Message (0xc)
        0000 .... = Reserved: 0
        .... 0010 = versionPTP: 2
        messageLength: 54
        subdomainNumber: 0
        Reserved: 0
        flags: 0x0400
        0... .... .... .... = PTP_SECURITY: False
        .0.. .... .... .... = PTP profile Specific 2: False
        ..0. .... .... .... = PTP profile Specific 1: False
        .... .1.. .... .... = PTP_UNICAST: True
        .... ..0. .... .... = PTP_TWO_STEP: False
        .... ...0 .... .... = PTP_ALTERNATE_MASTER: False
        .... .... ..0. .... = FREQUENCY_TRACEABLE: False
        .... .... ...0 .... = TIME_TRACEABLE: False
        .... .... .... 0... = PTP_TIMESCALE: False
        .... .... .... .0.. = PTP_UTC_REASONABLE: False
        .... .... .... ..0. = PTP_LI_59: False
        .... .... .... ...0 = PTP_LI_61: False
        correction: 0.000000 nanoseconds
        correction: Ns: 0 nanoseconds
        correctionSubNs: 0 nanoseconds
        Reserved: 0
        ClockIdentity: 0x08b258fffee2d7d0
```

```
        MAC Vendor: JuniperN
        SourcePortID: 1
        sequenceId: 89
        control: Other Message (5)
        logMessagePeriod: 127
        targetPortIdentity: 0xffffffffffffffff
        targetPortId: 65535
        tlvType: Request unicast transmission (4)
        lengthField: 6
        1001 .... = messageType: Delay_Resp Message (0x9)
        logInterMessagePeriod: -4
        period: every 0.0625 seconds
        rate: 16 packets/sec
        durationField: 300 seconds
```

Signalling Grant for DELAY-RESPONSE Packet

```
Frame 1: 102 bytes on wire (816 bits)
        Encapsulation type: Ethernet (1)
        Arrival Time: Jul 26, 2020 11:05:57.000000000 CEST
        Time shift for this packet: 0.000000000 seconds
        Epoch Time: 1595754357.000000000 seconds
        Time delta from previous captured frame: 0.000000000 seconds
        Time delta from previous displayed frame: 0.000000000 seconds
        Time since reference or first frame: 0.000000000 seconds
        Frame Number: 1
        Frame Length: 102 bytes (816 bits)
        Capture Length: 102 bytes (816 bits)
        Frame is marked: False
        Frame is ignored: False
        Protocols in frame: eth:ethertype:ip:udp:ptp
Ethernet II
        Destination: JuniperN_e2:d0:32 (08:b2:58:e2:d0:32)
        Address: JuniperN_e2:d0:32 (08:b2:58:e2:d0:32)
        .... ..0. .... .... .... .... = LG bit: Globally unique address (factory default)
        .... ...0 .... .... .... .... = IG bit: Individual address (unicast)
        Source: a0:00:00:00:00:01 (a0:00:00:00:00:01)
        Address: a0:00:00:00:00:01 (a0:00:00:00:00:01)
        .... ..0. .... .... .... .... = LG bit: Globally unique address (factory default)
        .... ...0 .... .... .... .... = IG bit: Individual address (unicast)
        Type: IPv4 (0x0800)
        Frame check sequence: 0xc4015466
        FCS Status: Unverified
Internet Protocol Version 4
        0100 .... = Version: 4
        .... 0101 = Header Length: 20 bytes (5)
        Differentiated Services Field: 0xb8 (DSCP: EF PHB, ECN: Not-ECT)
        1011 10.. = Differentiated Services Codepoint: Expedited Forwarding (46)
        .... ..00 = Explicit Congestion Notification: Not ECN-Capable Transport (0)
        Total Length: 84
        Identification: 0x0000 (0)
        Flags: 0x4000, Don't fragment
        0... .... .... .... = Reserved bit: Not set
        .1.. .... .... .... = Don't fragment: Set
        ..0. .... .... .... = More fragments: Not set
        Fragment offset: 0
        Time to live: 64
        Protocol: UDP (17)
        Header checksum: 0x25df
        Header checksum status: Unverified
        Source: 10.0.0.1
        Destination: 10.0.0.2
User Datagram Protocol
        Source Port: 320
        Destination Port: 320
        Length: 64
        Checksum: [missing]
        Checksum Status: Not present
        Stream index: 0
```

```
        Timestamps
        Time since first frame: 0.000000000 seconds
        Time since previous frame: 0.000000000 seconds
Precision Time Protocol (IEEE1588)
        0000 .... = transportSpecific: 0x0
        ...0 .... = V1 Compatibility: False
        .... 1100 = messageId: Signalling Message (0xc)
        0000 .... = Reserved: 0
        .... 0010 = versionPTP: 2
        messageLength: 56
        subdomainNumber: 0
        Reserved: 0
        flags: 0x0400
        0... .... .... .... = PTP_SECURITY: False
        .0.. .... .... .... = PTP profile Specific 2: False
        ..0. .... .... .... = PTP profile Specific 1: False
        .... .1.. .... .... = PTP_UNICAST: True
        .... ..0. .... .... = PTP_TWO_STEP: False
        .... ...0 .... .... = PTP_ALTERNATE_MASTER: False
        .... .... ..0. .... = FREQUENCY_TRACEABLE: False
        .... .... ...0 .... = TIME_TRACEABLE: False
        .... .... .... 0... = PTP_TIMESCALE: False
        .... .... .... .0.. = PTP_UTC_REASONABLE: False
        .... .... .... ..0. = PTP_LI_59: False
        .... .... .... ...0 = PTP_LI_61: False
        correction: 0.000000 nanoseconds
        correction: Ns: 0 nanoseconds
        correctionSubNs: 0 nanoseconds
        Reserved: 0
        ClockIdentity: 0x0000000000000001
        SourcePortID: 1
        sequenceId: 89
        control: Other Message (5)
        logMessagePeriod: 127
        targetPortIdentity: 0x08b258fffee2d7d0
        targetPortId: 1
        tlvType: Grant unicast transmission (5)
        lengthField: 8
        1001 .... = messageType: Delay_Resp Message (0x9)
        logInterMessagePeriod: -4
        period: every 0.0625 seconds
        rate: 16 packets/sec
        durationField: 300 seconds
        .... ...1 = renewalInvited: True
```

ANNOUNCE Packet

```
Frame 1: 110 bytes on wire (880 bits)
        Encapsulation type: Ethernet (1)
        Arrival Time: Jul 26, 2020 09:59:21.000000000 CEST
        Time shift for this packet: 0.000000000 seconds
        Epoch Time: 1595750361.000000000 seconds
        Time delta from previous captured frame: 0.000000000 seconds
        Time delta from previous displayed frame: 0.000000000 seconds
        Time since reference or first frame: 0.000000000 seconds
        Frame Number: 1
        Frame Length: 110 bytes (880 bits)
        Capture Length: 110 bytes (880 bits)
        Frame is marked: False
        Frame is ignored: False
        Protocols in frame: eth:ethertype:ip:udp:ptp
Ethernet II
        Destination: JuniperN_e2:d0:32 (08:b2:58:e2:d0:32)
        Address: JuniperN_e2:d0:32 (08:b2:58:e2:d0:32)
        .... ..0. .... .... .... .... = LG bit: Globally unique address (factory default)
        .... ...0 .... .... .... .... = IG bit: Individual address (unicast)
        Source: a0:00:00:00:00:01 (a0:00:00:00:00:01)
        Address: a0:00:00:00:00:01 (a0:00:00:00:00:01)
        .... ..0. .... .... .... .... = LG bit: Globally unique address (factory default)
```

```
        .... ...0 .... .... .... .... = IG bit: Individual address (unicast)
        Type: IPv4 (0x0800)
        Frame check sequence: 0x57482bb5
        FCS Status: Unverified
Internet Protocol Version 4
        0100 .... = Version: 4
        .... 0101 = Header Length: 20 bytes (5)
        Differentiated Services Field: 0xb8 (DSCP: EF PHB, ECN: Not-ECT)
        1011 10.. = Differentiated Services Codepoint: Expedited Forwarding (46)
        .... ..00 = Explicit Congestion Notification: Not ECN-Capable Transport (0)
        Total Length: 92
        Identification: 0x0000 (0)
        Flags: 0x4000, Don't fragment
        0... .... .... .... = Reserved bit: Not set
        .1.. .... .... .... = Don't fragment: Set
        ..0. .... .... .... = More fragments: Not set
        Fragment offset: 0
        Time to live: 64
        Protocol: UDP (17)
        Header checksum: 0x25d7
        Header checksum status: Unverified
        Source: 10.0.0.1
        Destination: 10.0.0.2
User Datagram Protocol
        Source Port: 320
        Destination Port: 320
        Length: 72
        Checksum: [missing]
        Checksum Status: Not present
        Stream index: 0
        Timestamps
        Time since first frame: 0.000000000 seconds
        Time since previous frame: 0.000000000 seconds
Precision Time Protocol (IEEE1588)
        0000 .... = transportSpecific: 0x0
        ...0 .... = V1 Compatibility: False
        .... 1011 = messageId: Announce Message (0xb)
        0000 .... = Reserved: 0
        .... 0010 = versionPTP: 2
        messageLength: 64
        subdomainNumber: 0
        Reserved: 0
        flags: 0x043c
        0... .... .... .... = PTP_SECURITY: False
        .0.. .... .... .... = PTP profile Specific 2: False
        ..0. .... .... .... = PTP profile Specific 1: False
        .... .1.. .... .... = PTP_UNICAST: True
        .... ..0. .... .... = PTP_TWO_STEP: False
        .... ...0 .... .... = PTP_ALTERNATE_MASTER: False
        .... .... ..1. .... = FREQUENCY_TRACEABLE: True
        .... .... ...1 .... = TIME_TRACEABLE: True
        .... .... .... 1... = PTP_TIMESCALE: True
        .... .... .... .1.. = PTP_UTC_REASONABLE: True
        .... .... .... ..0. = PTP_LI_59: False
        .... .... .... ...0 = PTP_LI_61: False
        correction: 0.000000 nanoseconds
        correction: Ns: 0 nanoseconds
        correctionSubNs: 0 nanoseconds
        Reserved: 0
        ClockIdentity: 0x0000000000000001
        SourcePortID: 1
        sequenceId: 0
        control: Other Message (5)
        logMessagePeriod: 1
        originTimestamp (seconds): 0
        originTimestamp (nanoseconds): 0
        originCurrentUTCOffset: 37
        priority1: 0
        grandmasterClockClass: 6
```

```
        grandmasterClockAccuracy: The time is accurate to within 25 ns (0x20)
        grandmasterClockVariance: 0
        priority2: 0
        grandmasterClockIdentity: 0x0000000000000001
        localStepsRemoved: 0
        TimeSource: ATOMIC_CLOCK (0x10)
```

SYNC Packet

```
Frame 1: 90 bytes on wire (720 bits)
        Encapsulation type: Ethernet (1)
        Arrival Time: Jul 26, 2020 10:02:40.000000000 CEST
        Time shift for this packet: 0.000000000 seconds
        Epoch Time: 1595750560.000000000 seconds
        Time delta from previous captured frame: 0.000000000 seconds
        Time delta from previous displayed frame: 0.000000000 seconds
        Time since reference or first frame: 0.000000000 seconds
        Frame Number: 1
        Frame Length: 90 bytes (720 bits)
        Capture Length: 90 bytes (720 bits)
        Frame is marked: False
        Frame is ignored: False
        Protocols in frame: eth:ethertype:ip:udp:ptp
Ethernet II
        Destination: JuniperN_e2:d0:32 (08:b2:58:e2:d0:32)
        Address: JuniperN_e2:d0:32 (08:b2:58:e2:d0:32)
        .... ..0. .... .... .... .... = LG bit: Globally unique address (factory default)
        .... ...0 .... .... .... .... = IG bit: Individual address (unicast)
        Source: a0:00:00:00:00:01 (a0:00:00:00:00:01)
        Address: a0:00:00:00:00:01 (a0:00:00:00:00:01)
        .... ..0. .... .... .... .... = LG bit: Globally unique address (factory default)
        .... ...0 .... .... .... .... = IG bit: Individual address (unicast)
        Type: IPv4 (0x0800)
        Frame check sequence: 0xe9b620be
        FCS Status: Unverified
Internet Protocol Version 4
        0100 .... = Version: 4
        .... 0101 = Header Length: 20 bytes (5)
        Differentiated Services Field: 0xb8 (DSCP: EF PHB, ECN: Not-ECT)
        1011 10.. = Differentiated Services Codepoint: Expedited Forwarding (46)
        .... ..00 = Explicit Congestion Notification: Not ECN-Capable Transport (0)
        Total Length: 72
        Identification: 0x0000 (0)
        Flags: 0x4000, Don't fragment
        0... .... .... .... = Reserved bit: Not set
        .1.. .... .... .... = Don't fragment: Set
        ..0. .... .... .... = More fragments: Not set
        Fragment offset: 0
        Time to live: 64
        Protocol: UDP (17)
        Header checksum: 0x25eb
        Header checksum status: Unverified
        Source: 10.0.0.1
        Destination: 10.0.0.2
User Datagram Protocol
        Source Port: 319
        Destination Port: 319
        Length: 52
        Checksum: [missing]
        Checksum Status: Not present
        Stream index: 0
        Timestamps
        Time since first frame: 0.000000000 seconds
        Time since previous frame: 0.000000000 seconds
Precision Time Protocol (IEEE1588)
        0000 .... = transportSpecific: 0x0
        ...0 .... = V1 Compatibility: False
        .... 0000 = messageId: Sync Message (0x0)
        0000 .... = Reserved: 0
```

```
        .... 0010 = versionPTP: 2
        messageLength: 44
        subdomainNumber: 0
        Reserved: 0
        flags: 0x0400
        0... .... .... .... = PTP_SECURITY: False
        .0.. .... .... .... = PTP profile Specific 2: False
        ..0. .... .... .... = PTP profile Specific 1: False
        .... .1.. .... .... = PTP_UNICAST: True
        .... ..0. .... .... = PTP_TWO_STEP: False
        .... ...0 .... .... = PTP_ALTERNATE_MASTER: False
        .... .... ..0. .... = FREQUENCY_TRACEABLE: False
        .... .... ...0 .... = TIME_TRACEABLE: False
        .... .... .... 0... = PTP_TIMESCALE: False
        .... .... .... .0.. = PTP_UTC_REASONABLE: False
        .... .... .... ..0. = PTP_LI_59: False
        .... .... .... ...0 = PTP_LI_61: False
        correction: 0.000000 nanoseconds
        correction: Ns: 0 nanoseconds
        correctionSubNs: 0 nanoseconds
        Reserved: 0
        ClockIdentity: 0x0000000000000001
        SourcePortID: 1
        sequenceId: 32921
        control: Sync Message (0)
        logMessagePeriod: 127
        originTimestamp (seconds): 1595748508
        originTimestamp (nanoseconds): 574961185
```

DELAY-REQUEST packet

```
Frame 1: 90 bytes on wire (720 bits)
        Encapsulation type: Ethernet (1)
        Arrival Time: Jul 26, 2020 10:04:29.000000000 CEST
        Time shift for this packet: 0.000000000 seconds
        Epoch Time: 1595750669.000000000 seconds
        Time delta from previous captured frame: 0.000000000 seconds
        Time delta from previous displayed frame: 0.000000000 seconds
        Time since reference or first frame: 0.000000000 seconds
        Frame Number: 1
        Frame Length: 90 bytes (720 bits)
        Capture Length: 90 bytes (720 bits)
        Frame is marked: False
        Frame is ignored: False
        Protocols in frame: eth:ethertype:ip:udp:ptp
Ethernet II
        Destination: a0:00:00:00:00:01 (a0:00:00:00:00:01)
        Address: a0:00:00:00:00:01 (a0:00:00:00:00:01)
        .... ..0. .... .... .... .... = LG bit: Globally unique address (factory default)
        .... ...0 .... .... .... .... = IG bit: Individual address (unicast)
        Source: JuniperN_e2:d0:32 (08:b2:58:e2:d0:32)
        Address: JuniperN_e2:d0:32 (08:b2:58:e2:d0:32)
        .... ..0. .... .... .... .... = LG bit: Globally unique address (factory default)
        .... ...0 .... .... .... .... = IG bit: Individual address (unicast)
        Type: IPv4 (0x0800)
        Frame check sequence: 0x1097e252
        FCS Status: Unverified
Internet Protocol Version 4
        0100 .... = Version: 4
        .... 0101 = Header Length: 20 bytes (5)
        Differentiated Services Field: 0xe0 (DSCP: CS7, ECN: Not-ECT)
        1110 00.. = Differentiated Services Codepoint: Class Selector 7 (56)
        .... ..00 = Explicit Congestion Notification: Not ECN-Capable Transport (0)
        Total Length: 72
        Identification: 0x0000 (0)
        Flags: 0x4000, Don't fragment
        0... .... .... .... = Reserved bit: Not set
        .1.. .... .... .... = Don't fragment: Set
        ..0. .... .... .... = More fragments: Not set
```

```
        Fragment offset: 0
        Time to live: 63
        Protocol: UDP (17)
        Header checksum: 0x26c3
        Header checksum status: Unverified
        Source: 10.0.0.2
        Destination: 10.0.0.1
User Datagram Protocol
        Source Port: 319
        Destination Port: 319
        Length: 52
        Checksum: [missing]
        Checksum Status: Not present
        Stream index: 0
        Timestamps
        Time since first frame: 0.000000000 seconds
        Time since previous frame: 0.000000000 seconds
Precision Time Protocol (IEEE1588)
        0000 .... = transportSpecific: 0x0
        ...0 .... = V1 Compatibility: False
        .... 0001 = messageId: Delay_Req Message (0x1)
        0000 .... = Reserved: 0
        .... 0010 = versionPTP: 2
        messageLength: 44
        subdomainNumber: 0
        Reserved: 0
        flags: 0x0400
        0... .... .... .... = PTP_SECURITY: False
        .0.. .... .... .... = PTP profile Specific 2: False
        ..0. .... .... .... = PTP profile Specific 1: False
        .... .1.. .... .... = PTP_UNICAST: True
        .... ..0. .... .... = PTP_TWO_STEP: False
        .... ...0 .... .... = PTP_ALTERNATE_MASTER: False
        .... .... ..0. .... = FREQUENCY_TRACEABLE: False
        .... .... ...0 .... = TIME_TRACEABLE: False
        .... .... .... 0... = PTP_TIMESCALE: False
        .... .... .... .0.. = PTP_UTC_REASONABLE: False
        .... .... .... ..0. = PTP_LI_59: False
        .... .... .... ...0 = PTP_LI_61: False
        correction: 13775.000015 nanoseconds
        correction: Ns: 13775 nanoseconds
        correctionSubNs: 1.52587890625e-05 nanoseconds
        Reserved: 0
        ClockIdentity: 0x08b258fffee2d7d0
        MAC Vendor: JuniperN
        SourcePortID: 1
        sequenceId: 61131
        control: Delay_Req Message (1)
        logMessagePeriod: 127
        originTimestamp (seconds): 1595748508
        originTimestamp (nanoseconds): 625788461
```

DELAY-RESPONSE Packet

```
Frame 1: 100 bytes on wire (800 bits)
        Encapsulation type: Ethernet (1)
        Arrival Time: Jul 26, 2020 10:06:13.000000000 CEST
        Time shift for this packet: 0.000000000 seconds
        Epoch Time: 1595750773.000000000 seconds
        Time delta from previous captured frame: 0.000000000 seconds
        Time delta from previous displayed frame: 0.000000000 seconds
        Time since reference or first frame: 0.000000000 seconds
        Frame Number: 1
        Frame Length: 100 bytes (800 bits)
        Capture Length: 100 bytes (800 bits)
        Frame is marked: False
        Frame is ignored: False
        Protocols in frame: eth:ethertype:ip:udp:ptp
Ethernet II
        Destination: JuniperN_e2:d0:32 (08:b2:58:e2:d0:32)
```

```
        Address: JuniperN_e2:d0:32 (08:b2:58:e2:d0:32)
        .... ..0. .... .... .... .... = LG bit: Globally unique address (factory default)
        .... ...0 .... .... .... .... = IG bit: Individual address (unicast)
        Source: a0:00:00:00:00:01 (a0:00:00:00:00:01)
        Address: a0:00:00:00:00:01 (a0:00:00:00:00:01)
        .... ..0. .... .... .... .... = LG bit: Globally unique address (factory default)
        .... ...0 .... .... .... .... = IG bit: Individual address (unicast)
        Type: IPv4 (0x0800)
        Frame check sequence: 0xd8d5d67b
        FCS Status: Unverified
Internet Protocol Version 4
        0100 .... = Version: 4
        .... 0101 = Header Length: 20 bytes (5)
        Differentiated Services Field: 0xe0 (DSCP: CS7, ECN: Not-ECT)
        1110 00.. = Differentiated Services Codepoint: Class Selector 7 (56)
        .... ..00 = Explicit Congestion Notification: Not ECN-Capable Transport (0)
        Total Length: 82
        Identification: 0x0000 (0)
        Flags: 0x4000, Don't fragment
        0... .... .... .... = Reserved bit: Not set
        .1.. .... .... .... = Don't fragment: Set
        ..0. .... .... .... = More fragments: Not set
        Fragment offset: 0
        Time to live: 32
        Protocol: UDP (17)
        Header checksum: 0x45b9
        Header checksum status: Unverified
        Source: 10.0.0.1
        Destination: 10.0.0.2
User Datagram Protocol
        Source Port: 320
        Destination Port: 320
        Length: 62
        Checksum: [missing]
        Checksum Status: Not present
        Stream index: 0
        Timestamps
        Time since first frame: 0.000000000 seconds
        Time since previous frame: 0.000000000 seconds
Precision Time Protocol (IEEE1588)
        0000 .... = transportSpecific: 0x0
        ...0 .... = V1 Compatibility: False
        .... 1001 = messageId: Delay_Resp Message (0x9)
        0000 .... = Reserved: 0
        .... 0010 = versionPTP: 2
        messageLength: 54
        subdomainNumber: 0
        Reserved: 0
        flags: 0x0400
        0... .... .... .... = PTP_SECURITY: False
        .0.. .... .... .... = PTP profile Specific 2: False
        ..0. .... .... .... = PTP profile Specific 1: False
        .... .1.. .... .... = PTP_UNICAST: True
        .... ..0. .... .... = PTP_TWO_STEP: False
        .... ...0 .... .... = PTP_ALTERNATE_MASTER: False
        .... .... ..0. .... = FREQUENCY_TRACEABLE: False
        .... .... ...0 .... = TIME_TRACEABLE: False
        .... .... .... 0... = PTP_TIMESCALE: False
        .... .... .... .0.. = PTP_UTC_REASONABLE: False
        .... .... .... ..0. = PTP_LI_59: False
        .... .... .... ...0 = PTP_LI_61: False
        correction: 13775.000015 nanoseconds
        correction: Ns: 13775 nanoseconds
        correctionSubNs: 1.52587890625e-05 nanoseconds
        Reserved: 0
        ClockIdentity: 0x0000000000000001
        SourcePortID: 1
        sequenceId: 61131
        control: Delay_Resp Message (3)
```

```
        logMessagePeriod: 127
        receiveTimestamp (seconds): 1595748508
        receiveTimestamp (nanoseconds): 625805285
        requestingSourcePortIdentity: 0x08b258fffee2d7d0
        requestingSourcePortId: 1
```

SyncE-Ethernet Synchronization Message Channel

ESMC Packet

```
Frame 1: 60 bytes on wire (480 bits)
        Encapsulation type: Ethernet (1)
        Arrival Time: Sep 22, 2020 07:34:28.000000000 CEST
        Time shift for this packet: 0.000000000 seconds
        Epoch Time: 1600752868.000000000 seconds
        Time delta from previous captured frame: 0.000000000 seconds
        Time delta from previous displayed frame: 0.000000000 seconds
        Time since reference or first frame: 0.000000000 seconds
        Frame Number: 1
        Frame Length: 60 bytes (480 bits)
        Capture Length: 60 bytes (480 bits)
        Frame is marked: False
        Frame is ignored: False
        Protocols in frame: eth:ethertype:slow:ossp:data
Ethernet II
        Destination: Slow-Protocols (01:80:c2:00:00:02)
        Address: Slow-Protocols (01:80:c2:00:00:02)
        .... ..0. .... .... .... .... = LG bit: Globally unique address (factory default)
        .... ...1 .... .... .... .... = IG bit: Group address (multicast/broadcast)
        Source: JuniperN_e2:d0:31 (08:b2:58:e2:d0:31)
        Address: JuniperN_e2:d0:31 (08:b2:58:e2:d0:31)
        .... ..0. .... .... .... .... = LG bit: Globally unique address (factory default)
        .... ...0 .... .... .... .... = IG bit: Individual address (unicast)
        Type: Slow Protocols (0x8809)
Slow Protocols
        Slow Protocols subtype: Organization Specific Slow Protocol (0x0a)
Organization Specific Slow Protocol
        OUI: 00:19:a7 (Itu-T)
        ITU-T OSSP Subtype: 0x0001: ESMC, Event:Information, QL-PRC
        0001 .... = Version: 0x1
        .... 0... = Event Flag: Information ESMC PDU (0x0)
        .... .0.. = Timestamp Valid Flag: Not set. Do not use Timestamp value even if Timestamp
        TLV present (0x0)
        Reserved: 0x0000000
        ESMC TLV, QL-PRC
        TLV Type: Quality Level (0x01)
        TLV Length: 0x0004
        0000 .... = Unused: 0x0
        .... 0010 = SSM Code: QL-PRC, Primary reference clock (G.811) (0x2)
        Padding: 00000000000000000000000000000000000000000000000000\xe2\x80\xa6, 32 octets
        Data ????
        Data: 00000000000000000000000000000000000000000000000000\xe2\x80\xa6
        Length: 32
```