JUNIPER NETWORKS | Engineering Simplicity

DAY ONE GREEN: JUNIPER ASIC TEAM PIONEERS SYSTEM-IN-PACKAGE (SIP) ASICS

Introducing the breathtaking abilities of Juniper's new System-in-Package design that increases key performance while using less power.

By Valery Kugel

Day One Green

Juniper ASIC Team Pioneers System-in-Package (SiP) ASICs

Juniper Networks was founded in 1996 and from day one began designing novel networking ASICs for internet traffic. During that quarter century, the company has designed more than 70 ASICs starting from 0.35um CMOS silicon technology (complementary metal–oxide–semiconductor) all the way to the most advanced CMOS nodes available today. This brief Day One Green paper looks to the future of Juniper ASIC design and the breathtaking abilities of the new System in Package (SiP) design that increases key performance while using less power.

The first Juniper ASICs had ~10 million transistors on a silicon die and a dozen 250Mbps high-speed IOs. The ASICs had silicon die area around 100-150mm2 and were packaged using small – 30-35mm on a side flip-chip organic substrate technologies, see Figure 1.

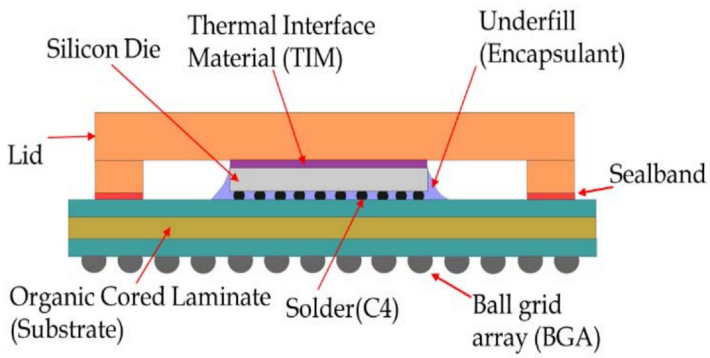

Figure 1 *A Typical Early Juniper ASIC in Flip-chip Package Assembly.*

With the advent of High Bandwidth Memory (HBM) in 2013, and then its second generation HBM2 in 2016, a new era of ASIC packing was introduced – integrating ASIC and HBMx on an ASIC package. It required a new packaging technology development to route very dense ASIC die-HBM interface signals. An example of such a technology is Taiwan Semiconductor Manufacturing Company's COWOS – Chip On Wafer On Substrate, see Figure 2. The ASIC die-HBM interface signals are routed on a silicon interposer, which is soldered to the package organic substrate using lead-free bumps. Juniper introduced HBM and the new packaging technology in both its Trio and Ex-press family.

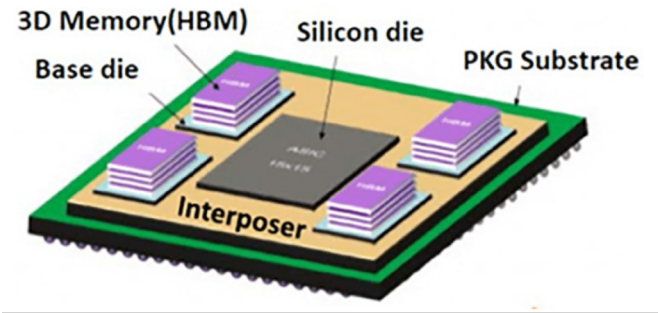

Figure 2 *Integrating HBM and ASIC Dies on a Package Substrate Using Silicon Interposer*

No doubt, the networking industry has experienced exponential increase in network bandwidth requirements during the last 25 years. The progress has translated to approximately doubling network equipment bandwidth every two years! While CMOS silicon technology was able to support bandwidth-hungry networking ASICs without significantly increasing the area and power of the ASICs for a long time, during the last ten

years there's been a gradual slowdown in CMOS silicon technology scaling. As a result, to support the bandwidth scaling requirements, the networking ASIC die's area grew significantly, see Figure 3. Together with the die area increase also grew the ASIC packages, which approached 60-70mm on a side.

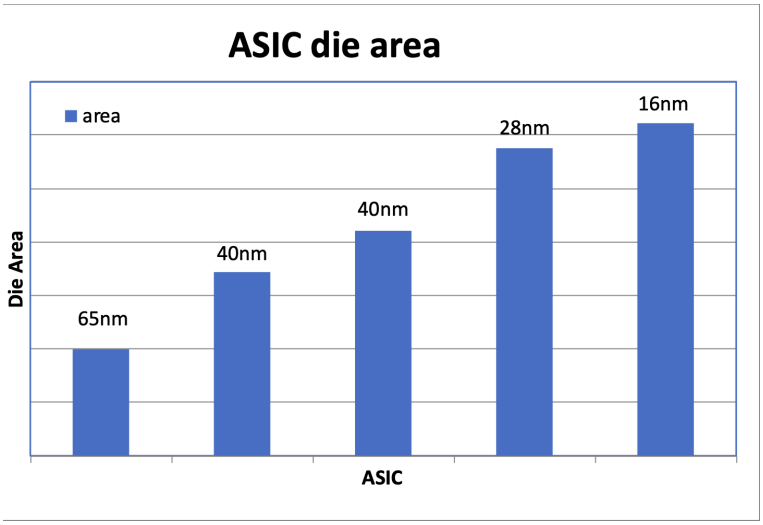

Figure 3 *Area Trends for Some Representative Juniper Networking ASICs*

And during the last five years we have observed a dramatic slowdown in CMOS technology scaling, so novel architectural approaches were required to keep scaling bandwidth of networking ASICs. Of prime importance has been Juniper ASIC team's pioneering System-in-Package (SiP) design approach using novel packaging technologies.

In Figure 4, two industry-leading routing Express ASICs are depicted. The ASICs have been discussed in detail by Dr. Chang-Hong Wu at the HotChips 2022 Conference (see References). Each 85mm x 85mm package has two networking ASIC dies (chiplets) and multiple HBMs; and each ASIC has two silicon interposers. X-chiplet has 59 billion transistors and the F-chiplet has 35 billion transistors! The ASIC chiplets communicate with each other using low-power SerDes macros designed to the CEI-112G-XSR-PAM4 standard, which Juniper co-sponsored at the OIF (Optical Internetworking Forum). This novel approach allows Juniper to design very complex SiPs in a cost- and energy-efficient manner.

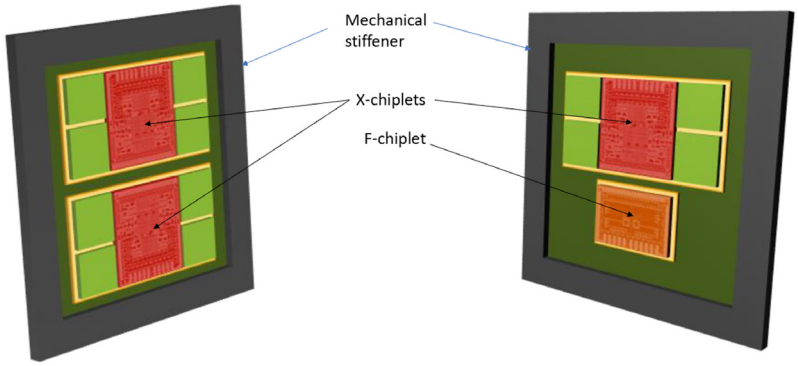

Figure 4 *28.8Tbps routing ASIC Designed Using Chiplet Approach.*

In conclusion, as seen in current trends in CMOS technology, the ability for Moore's law to deliver twice the networking bandwidth at the same cost and for the same die area and power is not there anymore. The Moore's law is de facto "stagnant." Therefore, the Juniper ASIC team has actively pursued novel architectures and technologies to continue delivering cutting edge networking ASICs with the lowest price and least power. We are also actively engaged with relevant standard organizations: IEEE, OIF, and more recently with UCIe consortium to make sure the standards incorporate requirements of the networking industry. Stay tuned for more exciting news from the Juniper ASIC team!

References

[1] Chang-Hong Wu, "Juniper's Express 5: A 28.8Tbps Network Routing ASIC and Variations" https://hc34.hotchips.org/assets/program/conference/day2/Network%20and%20Switches/HC2022.Juniper.ChangHong_Wu.v03.pdf

3100048-001-EN-Nov.2022