JUNIPER NETWORKS | Engineering Simplicity

DAY ONE GREEN:
IMPROVING NETWORK EFFICIENCY WITH ASIC ARCHITECTURE AND TECHNOLOGY

ASIC power consumption and heat dissipation are of paramount importance in today's networks.

By Chang-Hong Wu

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Improving Network Efficiency with ASIC Architecture and Technology

Every bit of information that passes through the network needs to be switched from its source to its destination somewhere along its path, usually multiple times by ASICs in networking systems. Therefore, ASIC power consumption and heat dissipation are of paramount importance in keeping the network efficient. Higher power and heat generation from ASICs also require more complex power supply and higher capacity fans for cooling, which themselves consume more power, further compounding the problem.

For many years, improvements in semiconductor fabrication technology kept delivering like clockwork. As captured by Gordon Moore in the famous Moore's law, semiconductor technology improved by roughly two times every eighteen months or so. If something was too costly, too hot, or too slow, you could just wait for the next generation of semiconductor fabrication technology, and essentially get a faster, cheaper, and lower-powered ASIC by riding the technology wave. There was still much hard work to do to better the networking systems in each generation but you also got the benefits from the new technologies themselves.

That's about exactly what happened during the first decade of this century and prior. Each successive generation of networking technology improved the bandwidth, functionality, and power by running the chips at higher speeds and with smaller number of chips, as illustrated in Figure 1. An example ASIC ran at about 156MHz at the beginning of the decade and ended at about 800MHz, greater than a five fold increase, while the number of ASICs comprising the chipsets reduced from ten down to two. It was the "the speed era" when we achieved higher bandwidth, better functionality, and lower power by running faster and in less total silicon area. By the end of the decade, Juniper introduced the Trio ASICs in the MX Universal Routing Platforms, a set of ASICs and systems that were so

flexible and programmable that they could support features required to not only run many of the networks at that point but for years to come, all at very high throughputs.

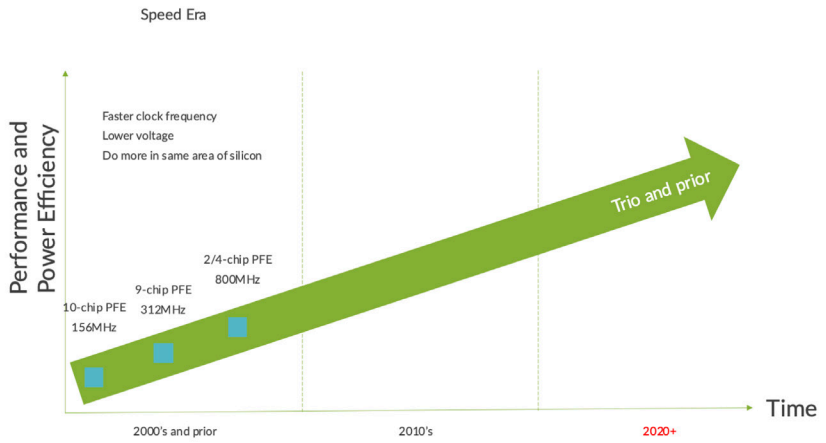

Figure 1: Decade of 2000's and Prior – Speed Era

By the latter half of the decade, though, the pace of semiconductor improvement was showing signs of slowing. While the density of logic still increased with each generation of the fabrication technology, the improvements in operating voltage, and therefore, intrinsic power consumption, basically slowed to a stop. By going to smaller and smaller geometries, the intrinsic transistor performance also stopped improving without adversely impacting its power consumption. This trend continued throughout the next decade, in the 2010's. In the meantime, with the increased popularity of video and the advent of mega data centers, the demand for bandwidth had never been greater, which put pressure on higher bandwidth and more power efficient networking products.

Here at Juniper we recognized that off-chip accesses by the ASICs were creating a bottleneck in achieving high bandwidths and they also consumed more power than on-chip connections. From these observations came the Express ASICs and the PTX core and transport routing platforms, with innovations such as Virtual Output Queuing and hash-based longest-prefix-match lookup techniques, which reduced off-chip packet buffer accesses by half and lookup accesses by roughly five times. As a result, by optimizing for the application areas of these networking products to the core and transport, and by using novel architectural techniques, we improved the power efficiency of the end products by roughly two times, in the same semiconductor technology, as depicted in Figure 2.

With the increase in bandwidth and interconnect among the chips, the power consumed by the interconnect made up a larger and larger percentage of the overall chipset power. Working with our industry partners, Juniper ASICs pioneered the use of 3D memories with high speed serial interfaces, enabling the integration of all the packet forwarding, queuing, and interfacing functions into a single chip. In the latter half of the decade (2010s), Juniper was among the first in networking vendors in adopting the in-package High Bandwidth Memory (HBM), further consolidating multiple slices and multiple processing cores onto the same dies. These innovative techniques reduced and eliminated much of the high power external interconnects, again producing higher bandwidth and more power efficient networking systems. The improvements made in the decade were mostly due to integration of more functions onto the same die, without much increase in logic speed; that's why I termed this decade as the "SOC era," or System on a Chip.

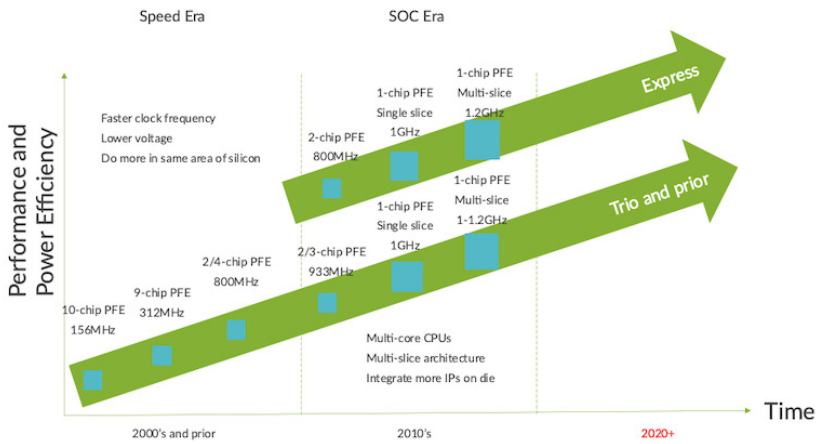

Figure 2: Decade of 2010's – SOC Era

The techniques used the "SOC era," however, resulted in larger and larger die size. In fact, by the end of the decade, many of the networking ASICs were approaching the maximum size that the current processing equipment could handle. In addition, in nanoscale semiconductor manufacturing, defects are naturally occurring phenomenon. Once the die size reaches a certain threshold, the probability of getting a defect-free chip from manufacturing decreases exponentially, thereby increasing the costs of a good product. Clearly, the SOC approach could not continue forever.

In recent years, the industry is embarking on a new approach, sometimes dubbed the "More than Moore" approach. Instead of using separate ASICs on the PCB (thus increasing the interconnect power), or putting everything on a single die (thus sacrificing costs), the idea is to put multiple reasonably-sized dies inside the same package, each in their optimized technology node, interconnected through lower power local interconnects. This way we can continue to increase the functionality of the systems and at the same time optimize the energy costs. This is likely the new approach for the 2020's. See Figure 3.

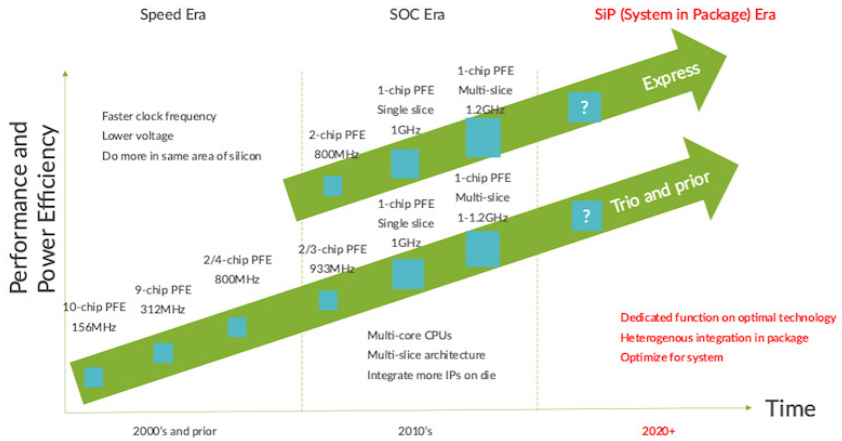

Figure 3: Decade of 2020+: System-in-Package Er

Juniper is continuing to come up with new architectural and integration techniques, working with our partners, and improving the economics and power efficiencies of our products in this new "SiP (System-in-a Package) era."

Watch this space for current breakthroughs on how Juniper is improving networking system power consumption with ASIC architecture and technology.

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