Silicon Photonics

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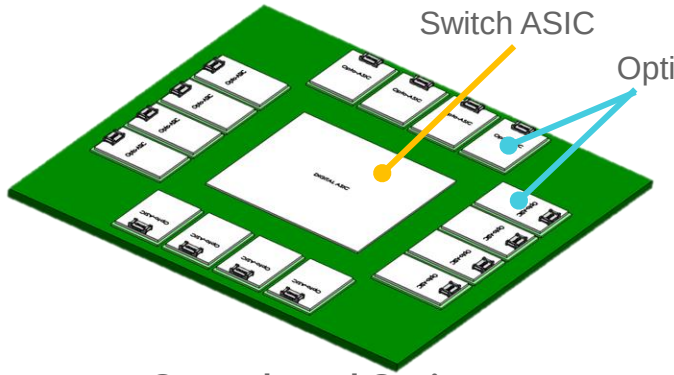
SILICON PHOTONICS

Vision = Optics manufactured like electronics

A scalable optical technology that is manufactured with the silicon electronics ecosystem (design, fabrication, packaging, and test) to enable high volume, low cost transceivers that can be co-packaged within larger electronic systems.



Co-packaged Optics

Reality today = Lower cost optics manufacturing

Optical components and assemblies that are manufactured using the silicon electronics manufacturing ecosystem. Transceivers utilize external lasers and fiber attach approaches that cannot survive reflow, limiting packaging to pluggable modules.

Pluggable Modules

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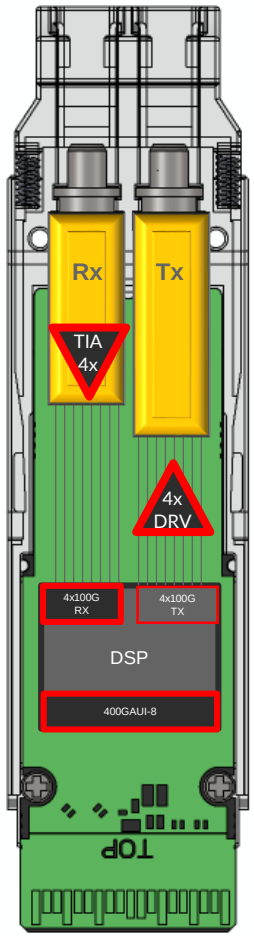
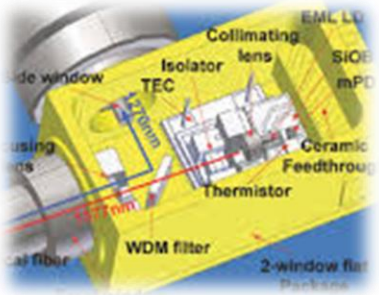
TECHNOLOGY COMPARISON

Conventional Optics



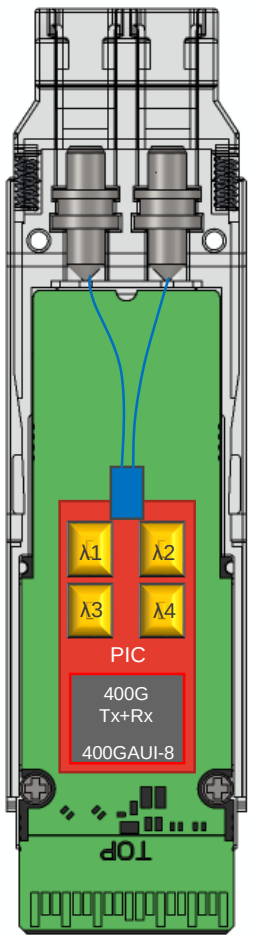
- Incumbent technology common in pluggable modules
- Discrete optical components



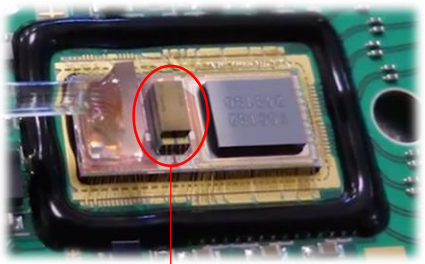
Transmitter Optical Subassembly

Labor Intensive

Silicon Photonics 1.0

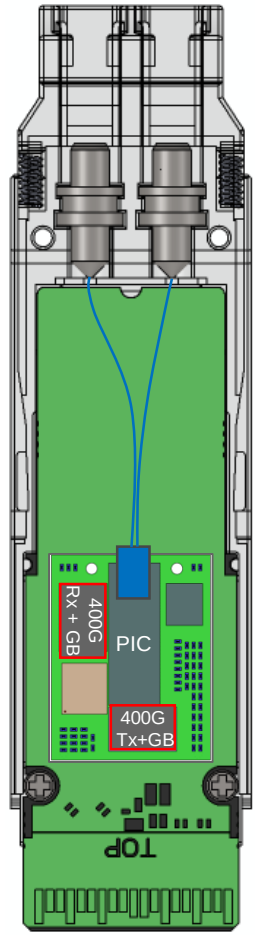


- Lasers are external to silicon photonics
- Most optical components integrated on silicon die

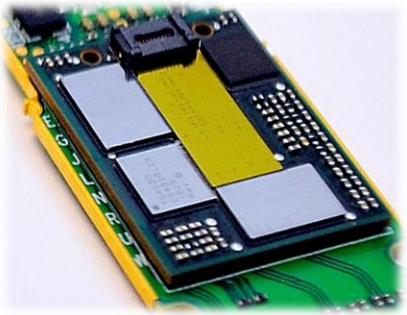


Si Photonics die with flip chipped electronics and external laser

Silicon Photonics 2.0



- Lasers integrated into the silicon die (**the holy grail!**)
- Only two companies capable of doing this.



System in package transceiver

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THE HOLY GRAIL

In terms of technology, the biggest elephant in the room is the lack of a silicon-photonics laser integrated in the chip to get data off quickly, Gartner said. "No one has developed that yet, and it is one of the holy grails of photonics."

Bill Gartner, Cisco VP/GM Optical Systems & Optics Group

Cooney, M. (2019, Feb 8) "Cisco pushes silicon photonics for enterprise, webscale networking", Retrieved from NetworkWorld.com

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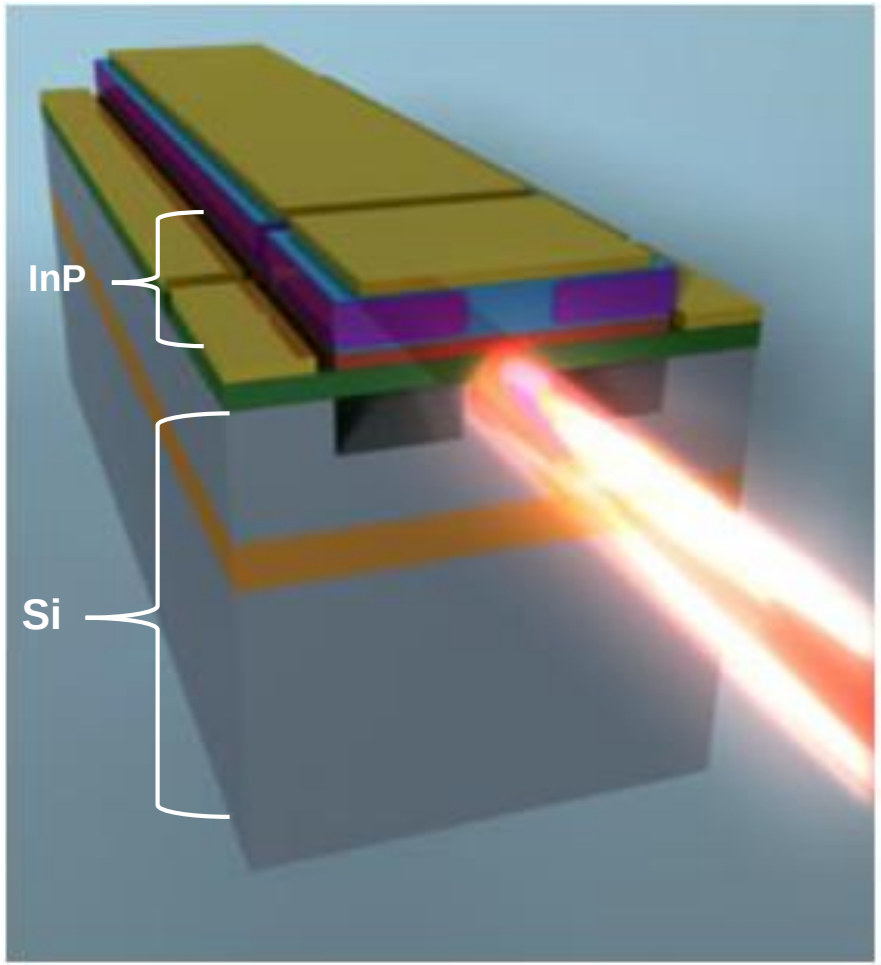
THE TALE OF TWO MATERIALS



Silicon (Si)

- Elemental material and abundant on earth
- A semiconductor - conducts electricity under some conditions, insulates electricity under others conditions
- Strong mechanical properties
- Can “guide” photons (light)
- But it can not generate photons (light) efficiently

Compound semiconductors

- Composed of elements from two or more different groups of the periodic table – ex: Indium + Phosphate (InP)
- Compound crystals are more difficult to grow than silicon
- The number of defects in the crystal is higher
- Wafers become fragile
- Cost of making the crystal is higher
- **But** can generate photons (light) efficiently

USE BOTH - InP Only Where Needed!

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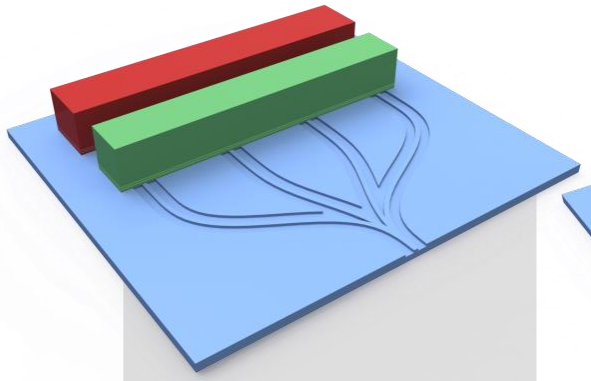
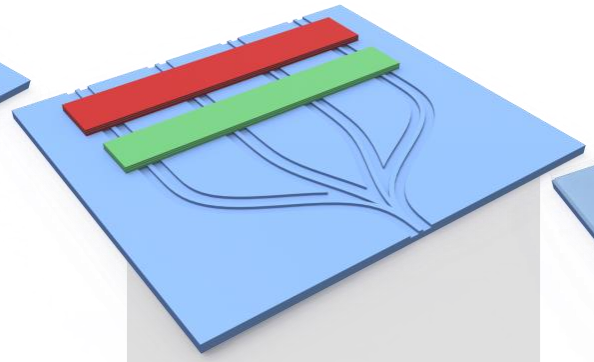
KEY TECHNOLOGY
INTEGRATING GAIN INTO A SILICON PROCESS



Die Placement

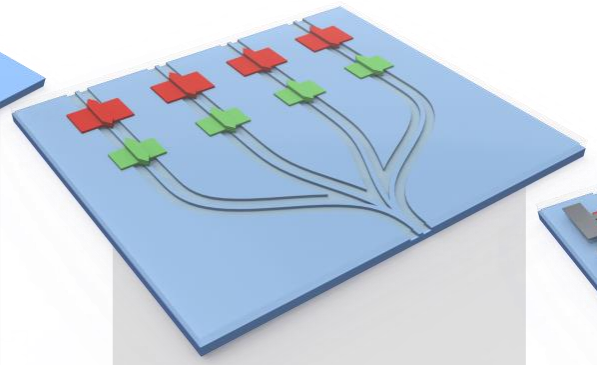
Mature silicon photonics passives

Integration of multiple III-V Materials



Substrate Removal

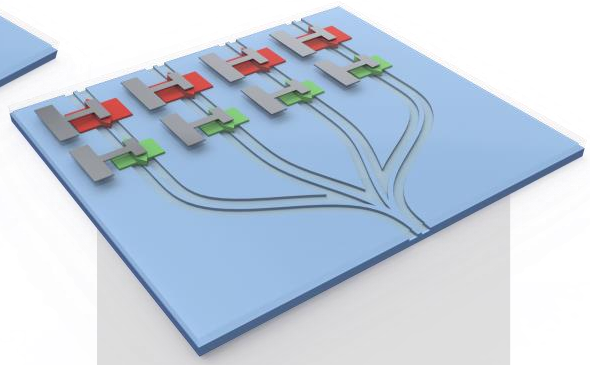
Reduced topology for Standard Processing



III-V Processing

Active materials defined by lithography

No critical alignment



Interconnect

Hermetic at Chip Scale

Wafer scale processing

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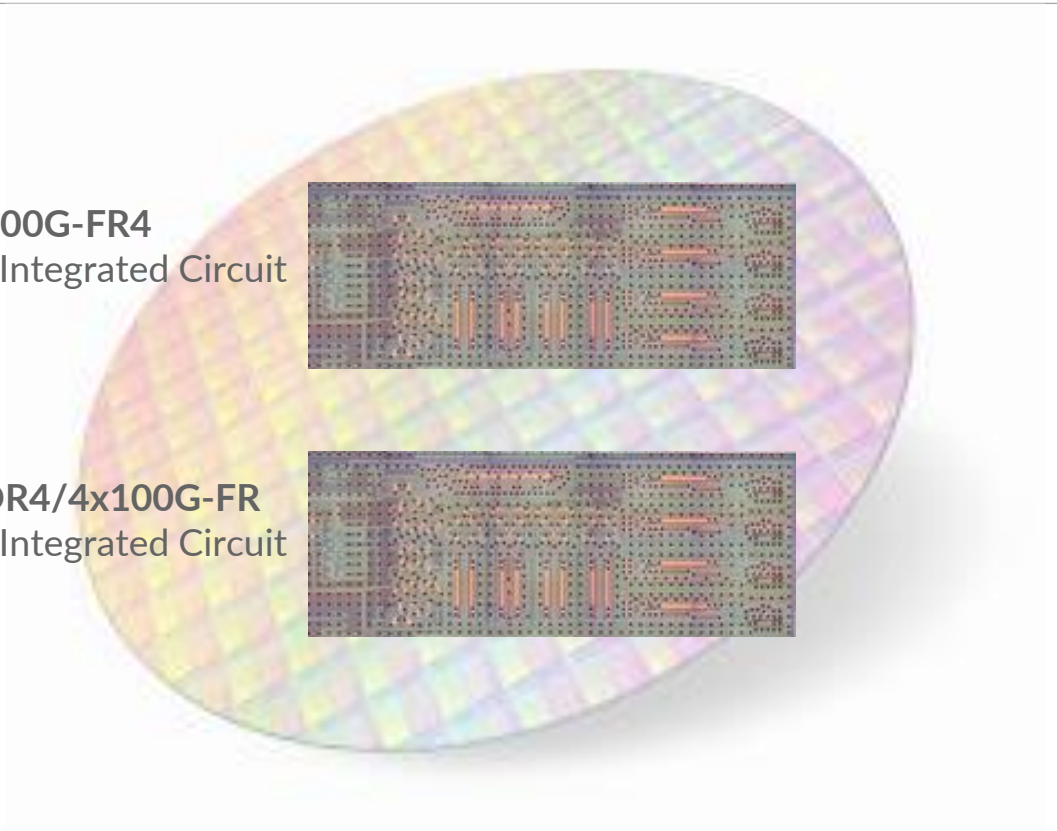
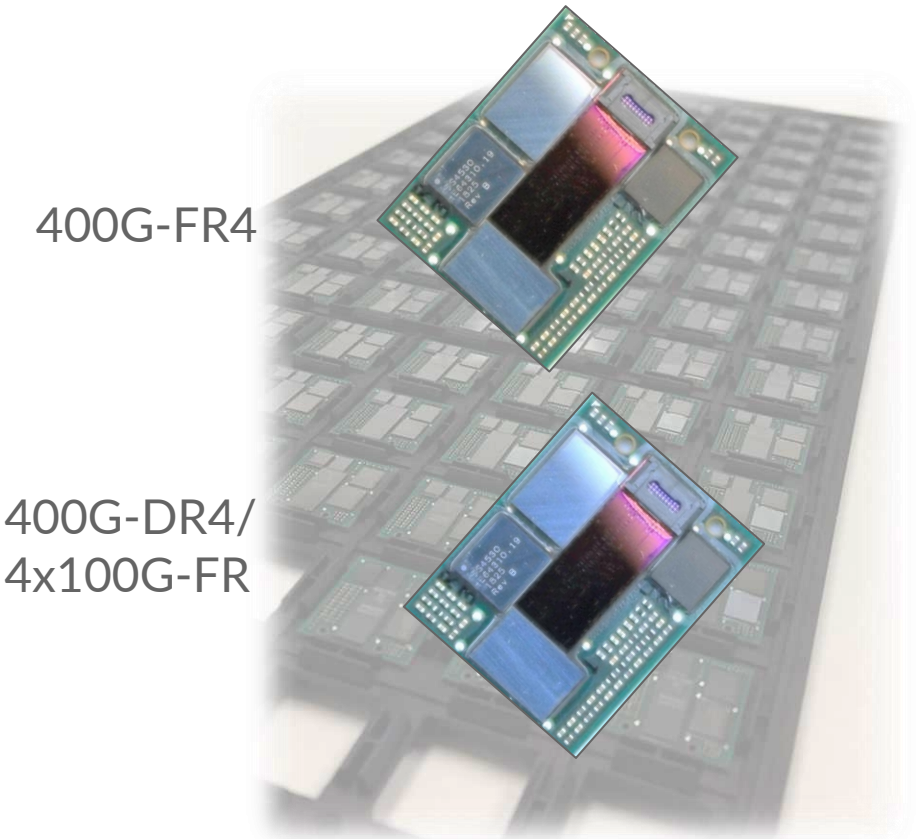
OPTICS MANUFACTURED LIKE ELECTRONICS





- **Entire optical Tx and Rx functionality in a single silicon die**
- **Fabless manufacturing in mainstream fabs**

- **Fully integrated transceiver in standard electronics based BGA package**
- **Standard microelectronics testing methods**

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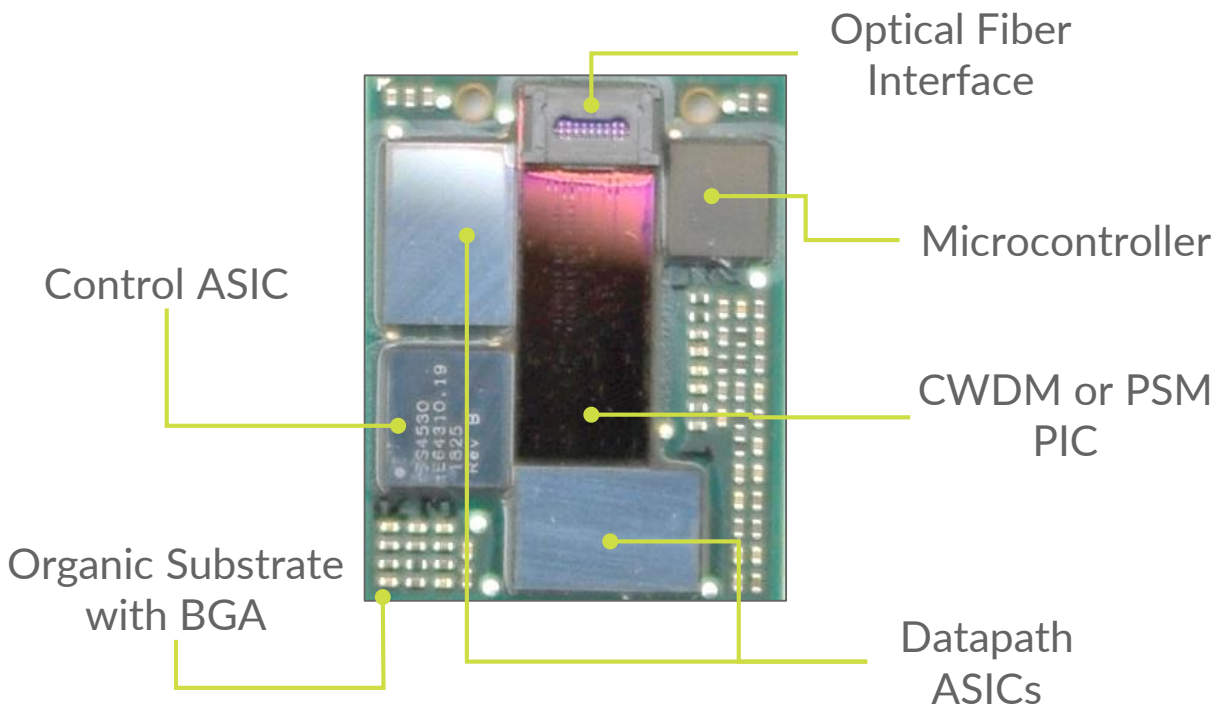
OPTO-ASIC

SYSTEM-IN-PACKAGE OPTICAL TRANSCEIVER ASIC

400G



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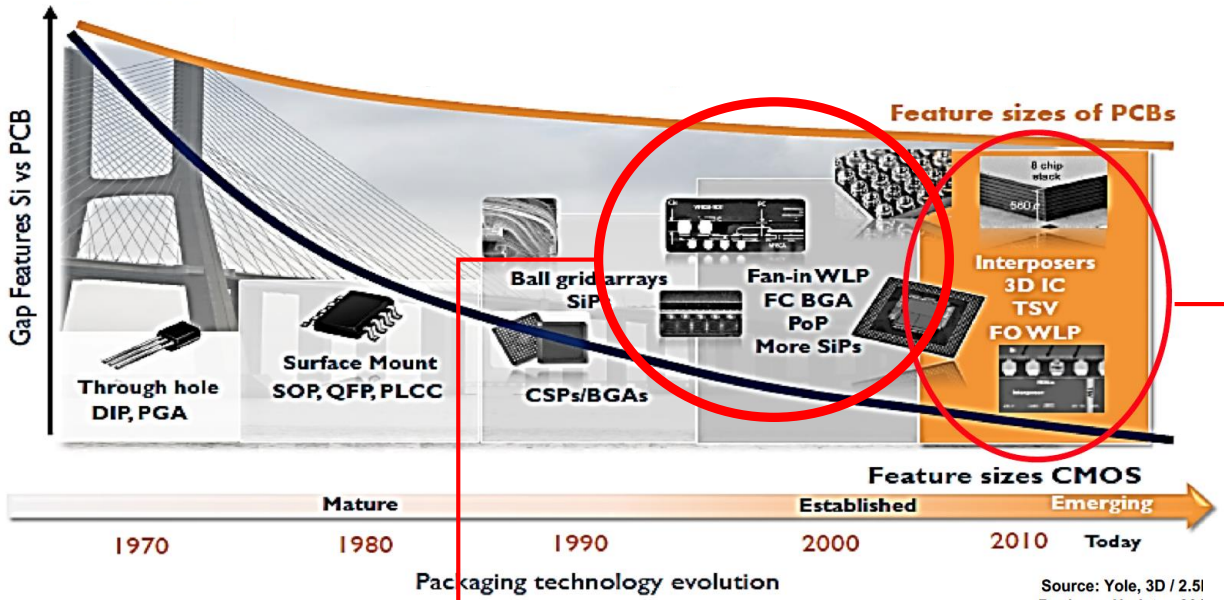
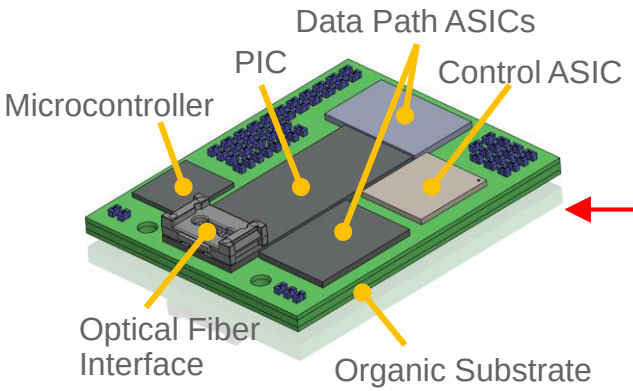
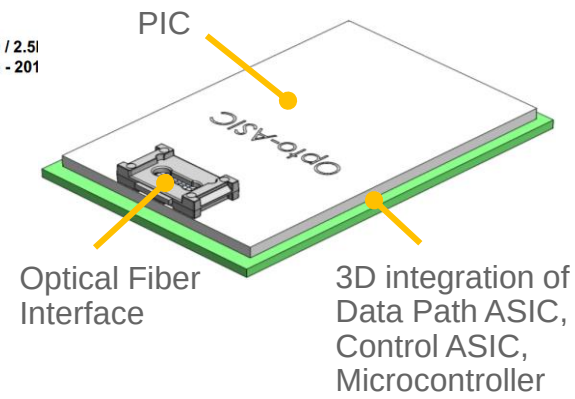
LEVERAGING MATURE LOW-COST PACKAGE TECHNOLOGY



400Gbps



3.2 Tbps



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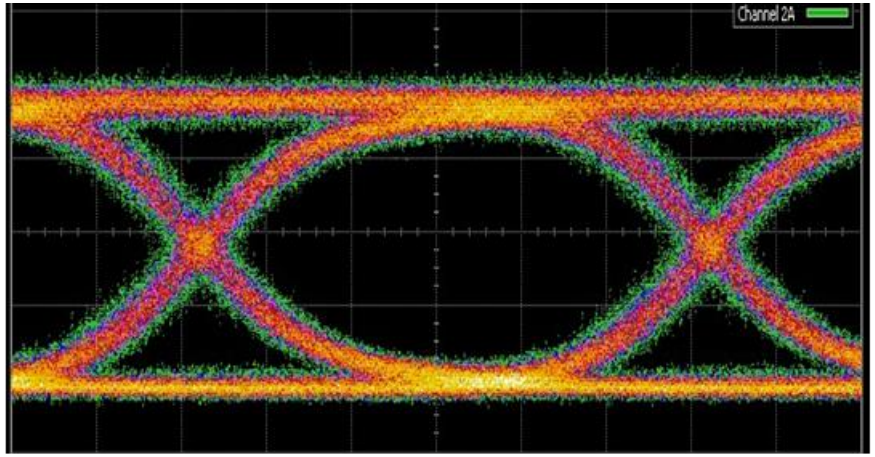
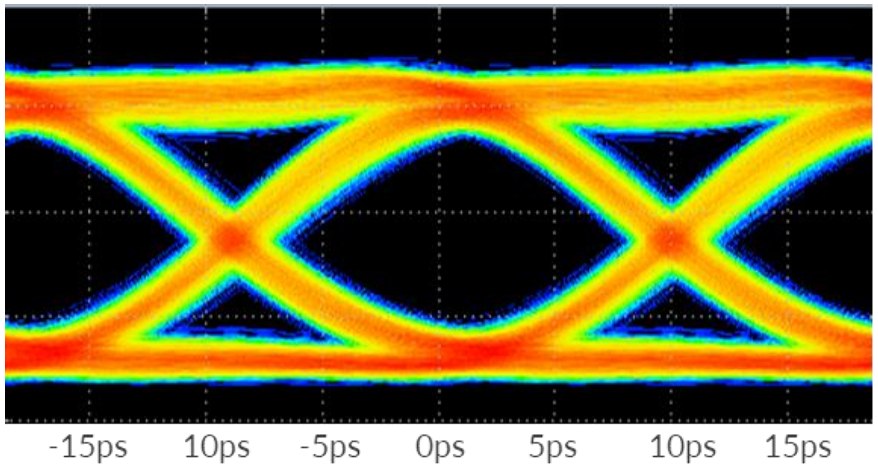
SCALABLE PERFORMANCE

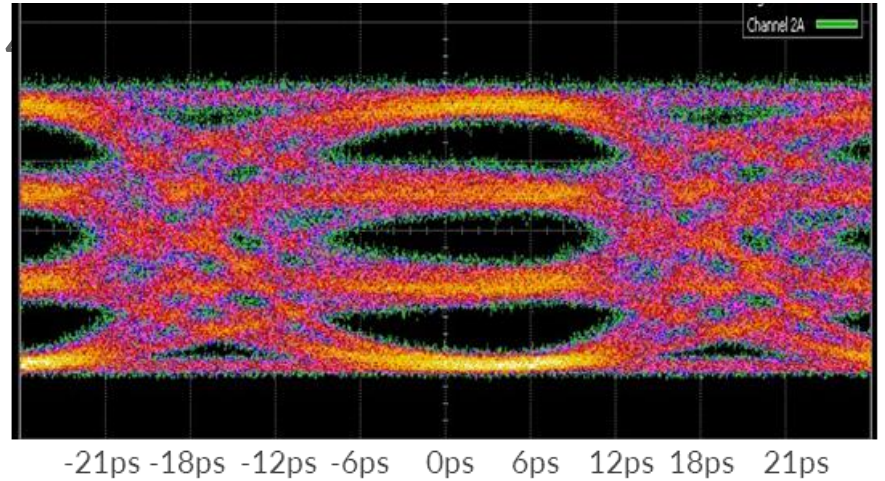
26G NRZ



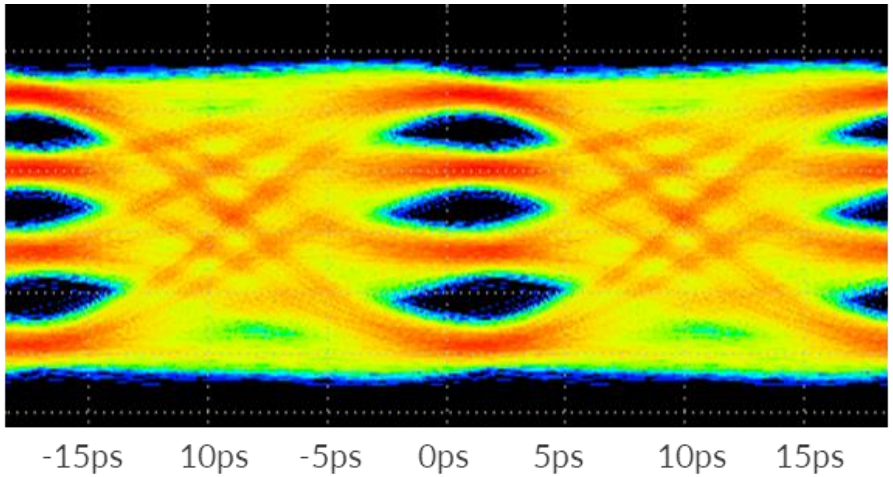
53G NRZ*



53G PAM4*



106G PAM4*



* Alpha Silicon

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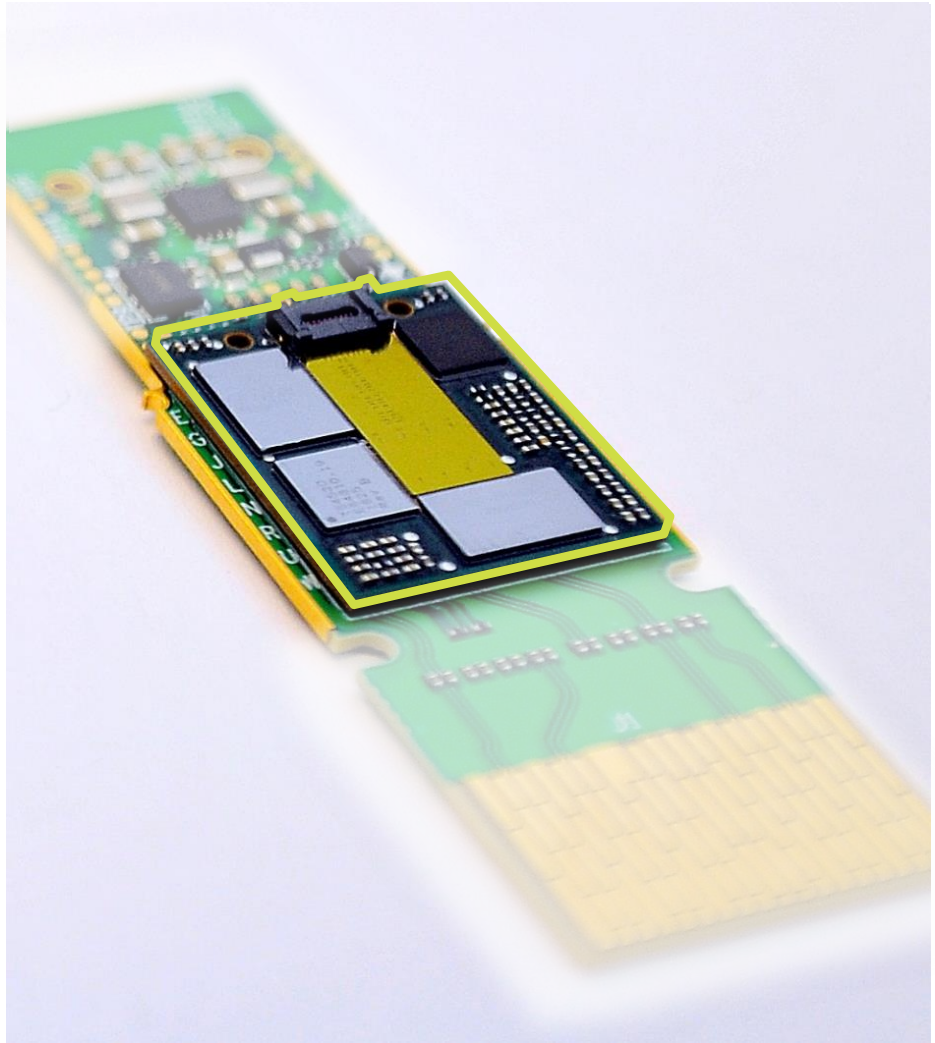
INTEGRATED TROUBLESHOOTING

Integrated Optical Loopback Switch Between TX and RX

- Optical verification during manufacturing
- Leverage functionality for in-service network diagnostics



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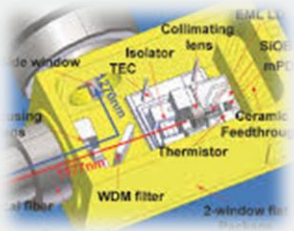
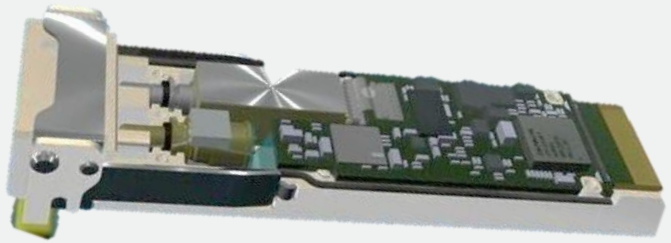
A NEW SUPPLY CHAIN FOR OPTICAL TRANSCEIVERS

Optics Manufacturing Today

Specialized Fabs

Labor Intensive





- Discrete manufacturing approaches
- Many different technologies – no economies of scale
- Transceiver designed to package

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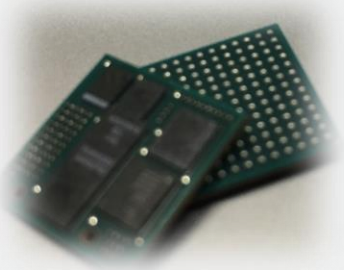
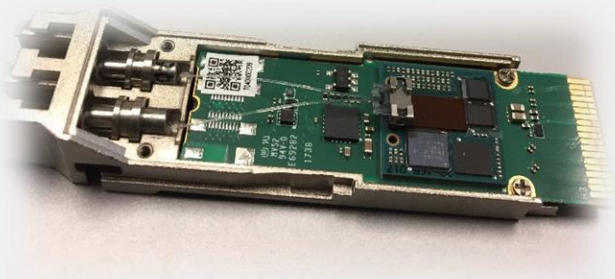
Silicon Fabs

Microelectronics Assembly & Test

Contract Manufacturers





- Utilizing the highly automated multi-billion dollar microelectronics ecosystem that is used across industries
- Transceiver agnostic to package

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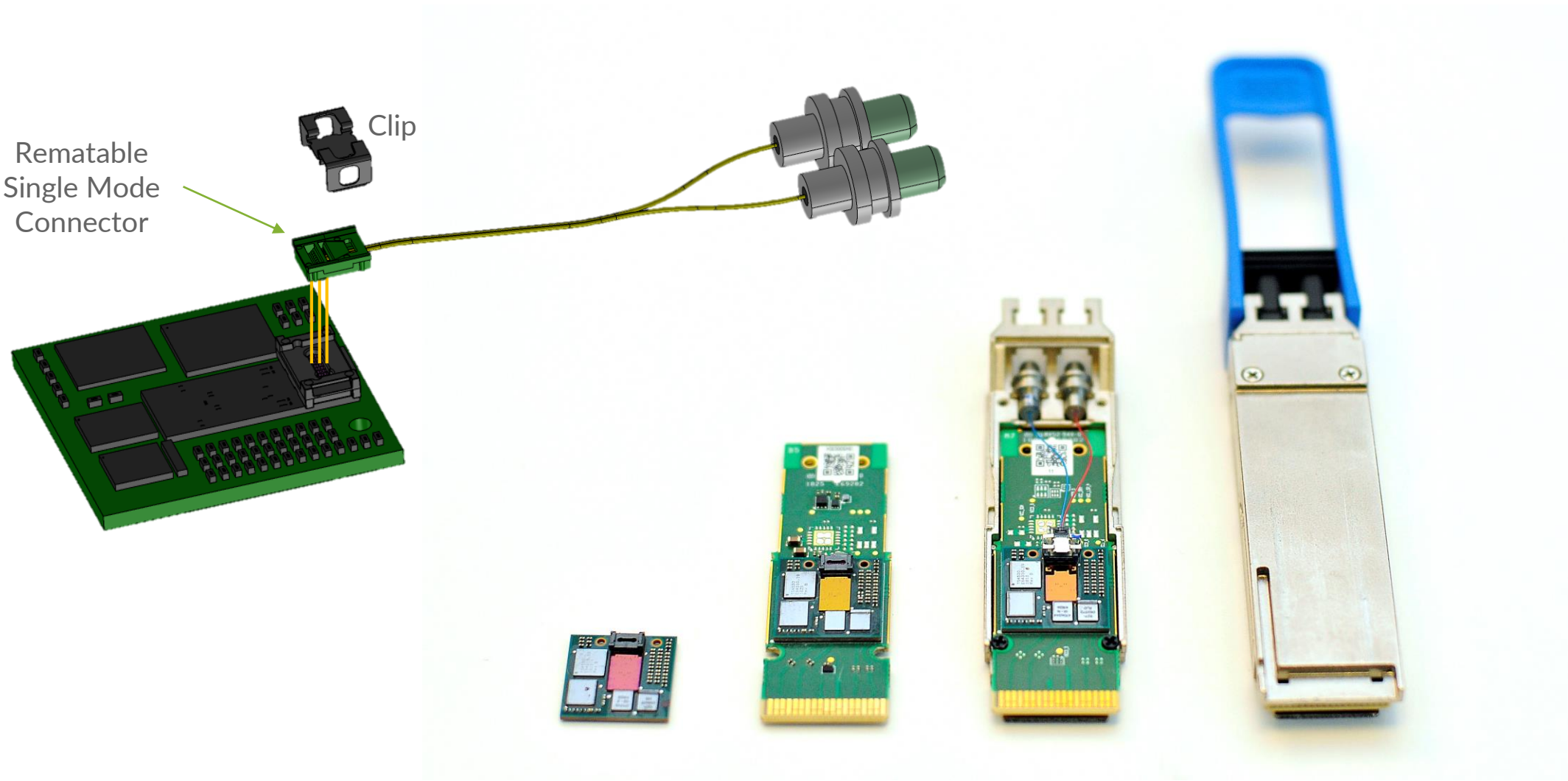
ENABLING STANDARD SURFACE MOUNT ASSEMBLY



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SILICON PHOTONICS PRODUCT OVERVIEW

100G

QSFP56-DD

- **4x100G-FR** (2km)
- Fiber Connector: 4xSN
- Power 7.8 Watts

400G

QSFP56-DD

- **400GBASE-DR4** (500m)
- Fiber Connector: MPO
- Power 7.8 Watts

QSFP56-DD

- **400G-FR4** (2km)
- Fiber Connector: LC
- Power 7.9 Watts

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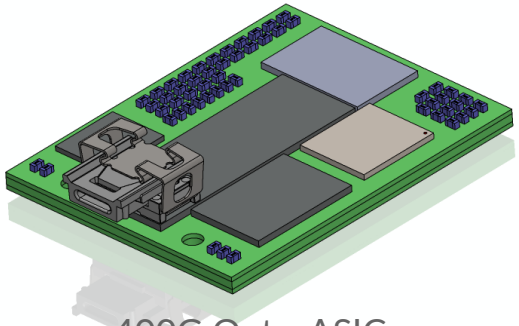
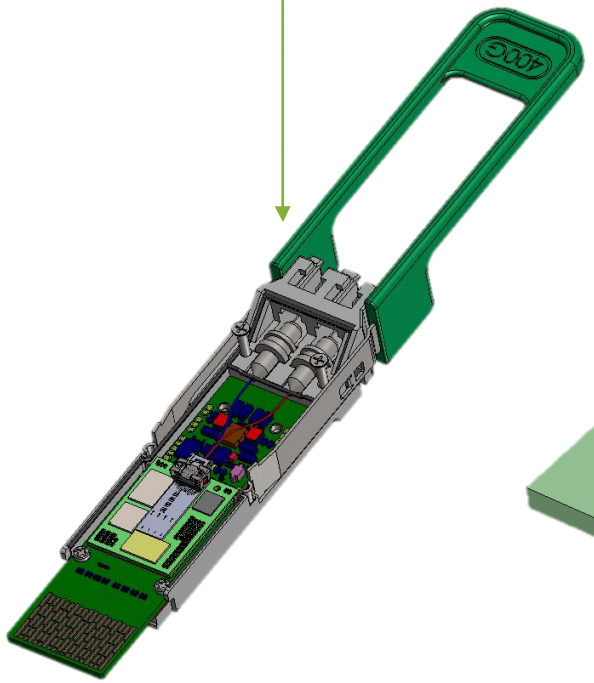
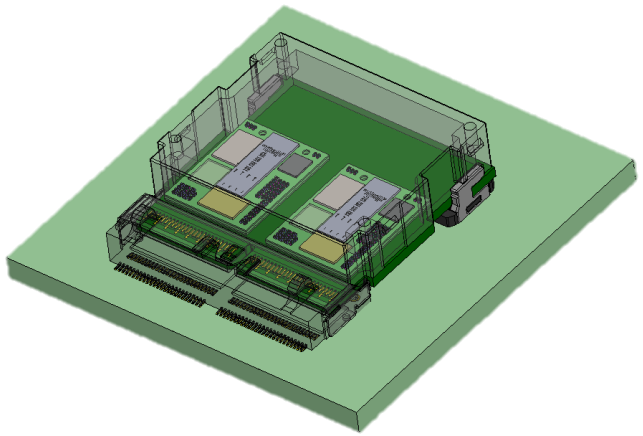
NO LIMIT TO FORM FACTOR



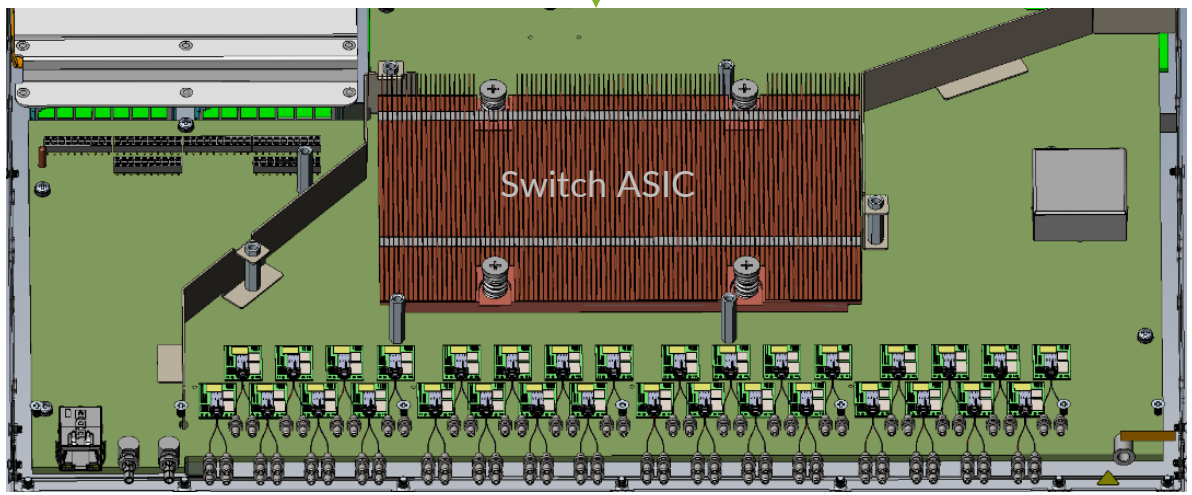
400G Opto-ASIC



400G
Pluggable Module



2x400G
COBO Module



32x400G
On-Board Opto-ASICs

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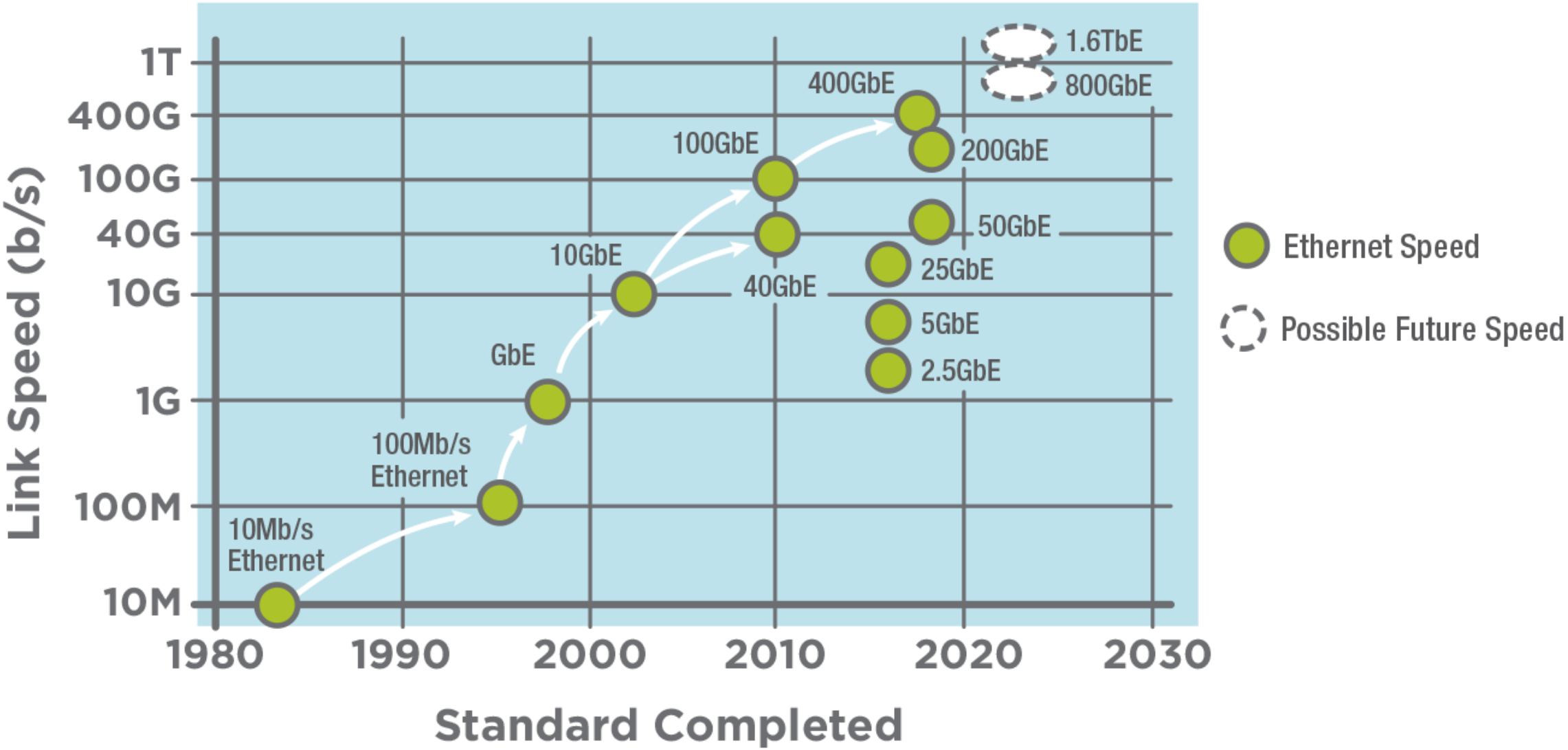
ETHERNET SPEEDS



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EVOLUTION OF NETWORKING SYSTEMS

Line Card or Switch Box

1. **Pluggable**: ASIC → PCB → SERDES→ Pluggable Connector → SERDES → TOSA/ROSA
2. **Pluggable**: ASIC → PCB → Pluggable Connector → SERDES → TOSA/ROSA
3. **Pluggable:** ASIC → PCB → Pluggable Connector → SERDES → PIC
4. **On-Board:** ASIC → PCB → SERDES → PIC
5. **Co-Packaged**: ASIC → PIC

Decreasing Power Consumption & Increasing BW Density

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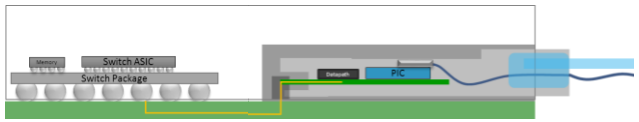
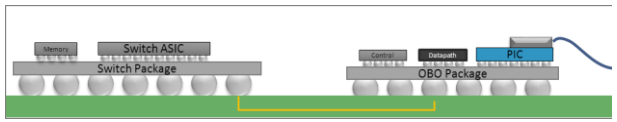
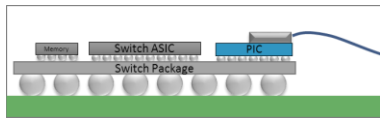
COMPARISON OF OPTICS PACKAGING APPROACHES







	Pluggable	On-Board Optics	Co-Package Optics
System Cost / Port	Highest	Medium to Low	Lowest
Density of Ports	Lowest	Medium to High	High
Power Consumption	Highest	Medium to High	Lowest
System BW per RU (limited by)	14.4T or 28.8T (faceplate area)	~40T (board area, thermal)	>75T (power, thermal)

On-Board and Co-Packaged Optics are needed to continue to meet future BW needs

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INDUSTRY IS GETTING SERIOUS ON CO-PACKAGED OPTICS

Microsoft and Facebook announce formation of the Co-Packaged Optics Collaboration under the Joint Development Foundation

Microsoft

Co-Packaged Optics Collaboration to focus on specifications for packaged integration of network-switching ASICs and optics

NEWS PROVIDED BY
Microsoft Corp. →
Mar 14, 2019, 14:00 ET

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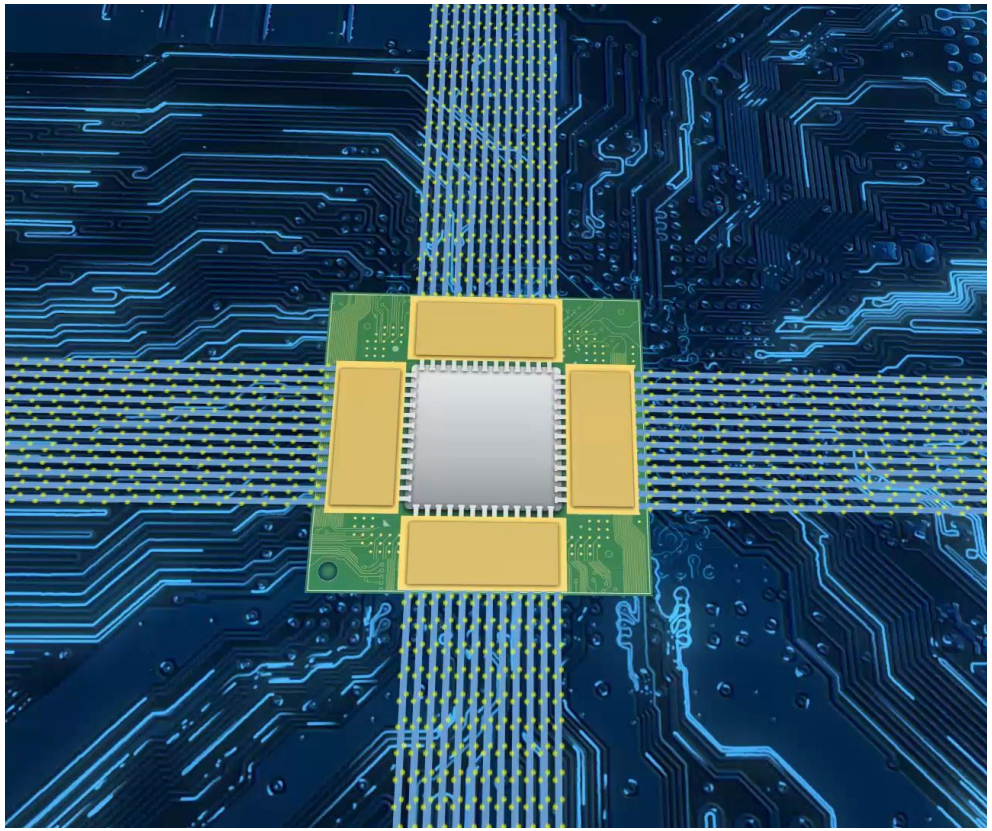
REDMOND, Wash. and MENLO PARK, Calif., March 14, 2019 /PRNewswire/ -- Datacenter architectures are growing at a rapid rate, and switch designs are evolving to support greater networking demands. Technical challenges associated with these demands have the potential to impact the adoption of future technologies if left unaddressed. Co-packaging optics and ASICs have the potential to address these challenges by reducing the length of the switch-optic interconnects, thus lowering the power consumption of the switch-optic electrical I/O.



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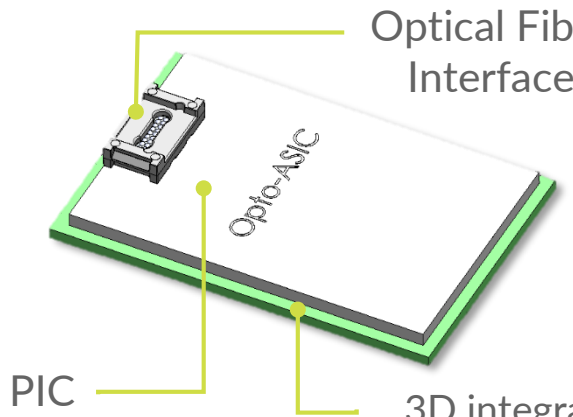
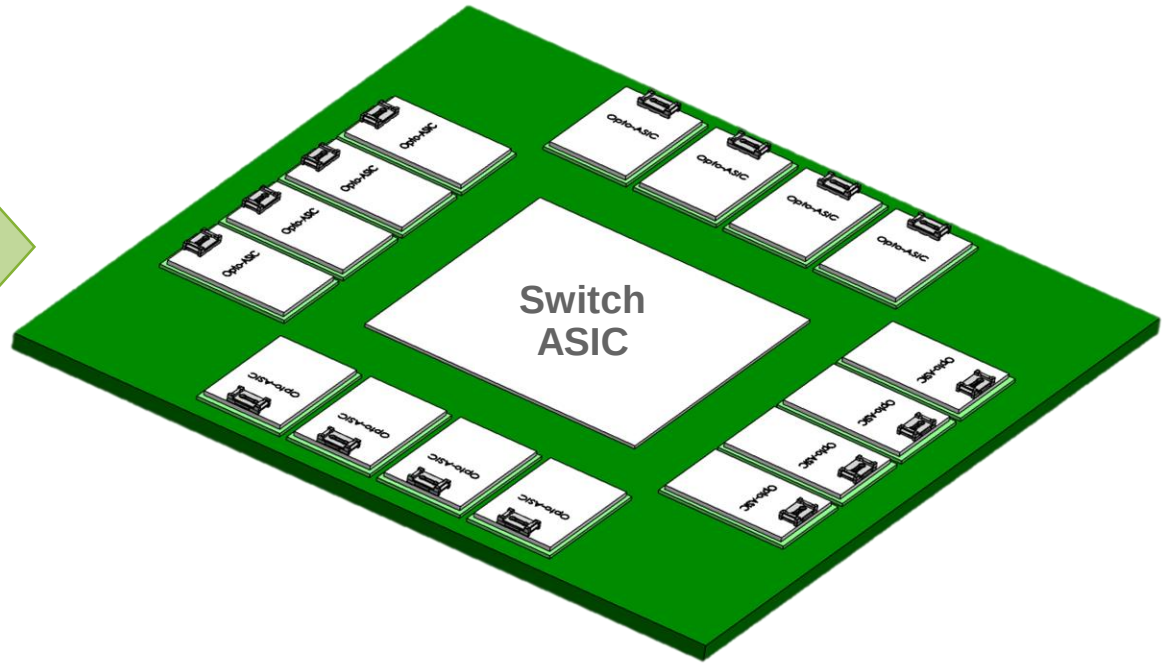
JUNIPER CO-PACKAGED OPTICS VISION

3.2 Tb/s Opto-ASIC Transceiver



Optical I/O:	8x 400G
Electrical I/O:	32x 112G-XSR

Co-Packaged Optics



Petabit-per-second System Switching Capacity

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