

Chapter 12

Channelized Interfaces Overview

Channelized interfaces enable you to configure a number of individual channels that subdivide the bandwidth of a larger interface and minimize the number of Physical Interface Cards (PICs) that an installation requires.



NOTE: Channelized intelligent queuing (IQ) interfaces require M-series Enhanced Flexible PIC Concentrators (FPCs).

Wherever JUNOS configuration guides refer to channelized interfaces and PICs without the “intelligent queuing” or “IQ” descriptor, they are referring to the original channelized interfaces and PICs.

For channelized IQ logical interfaces, you can configure class of service (CoS). For more information, see “Associating a Scheduler Map with a DLCI or VLAN” on page 846.

This chapter provides a high-level overview of channelized interfaces, focusing mainly on the capabilities, properties, and structure of channelized IQ interfaces:

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Channelized Interface Capabilities

You can configure each port of a channelized IQ PIC as a single interface that uses the entire available bandwidth, or partition each port into smaller data channels. In either case, you start with a channelized interface (designated by a *c* in the interface name, as in *coc12*). From the channelized interfaces, you configure data channels. Following are the channelized interface names and data-channel interface names associated with channelized IQ PICs.

Channelized Interface Names

coc12-fpc/pic/port—Channelized OC12 interface. Configure on a Channelized OC12 IQ PIC.

coc1-fpc/pic/port:channel—Channelized OC1 interface. Configure on a Channelized OC3 IQ PIC or Channelized OC12 IQ PIC.

ct3-fpc/pic/port<:channel>—Channelized T3 interface. Configure on a Channelized OC3 IQ, Channelized OC12 IQ, or Channelized DS3 IQ PIC.

cstm-1-fpc/pic/port—Channelized STM1 interface. Configure on a Channelized STM1 IQ PIC.

cau4-fpc/pic/port:channel—Channelized AU-4 IQ interface. Configure on a Channelized STM1 IQ PIC.

ct1-fpc/pic/port<:channel>—Channelized T1 interface. Configure on a Channelized OC3 IQ, Channelized OC12 IQ, or Channelized DS3 IQ PIC.

ce1-fpc/pic/port<:channel>—Channelized E1 interface. Configure on a Channelized E1 IQ or a Channelized STM1 IQ PIC.

Data-Channel Interface Names

e1-fpc/pic/port<:channel>—E1 channel. Configure on a Channelized E1 IQ or a Channelized STM1 IQ PIC.

ds-fpc/pic/port<:channel>—*N*xDS0 channel. Configure on a Channelized OC3 IQ, Channelized OC12 IQ, Channelized STM1 IQ, Channelized DS3 IQ, or Channelized E1 IQ PIC.

so-fpc/pic/port:channel—SONET/SDH channel. Configure one OC3 channel on a Channelized OC3 IQ, four OC3 channels on a Channelized OC12 IQ, one OC12 channel on a Channelized OC12 IQ, or one STM1 channel on a Channelized STM1 IQ PIC.

t1-fpc/pic/port<:channel>—T1 channel. Configure on a Channelized OC3 IQ or Channelized OC12 IQ or Channelized DS3 IQ PIC.

t3-fpc/pic/port<:channel>—T3 channel. Configure on a Channelized OC3 IQ, Channelized OC12 IQ, or Channelized DS3 IQ PIC.

Data-Link Connection Identifiers on Channelized Interfaces

If you use Frame Relay encapsulation on a channelized interface, see Table 22 for the maximum number of data-link connection identifiers (DLCIs) per channel that you can configure at each channel level for various channelized PICs.



NOTE: The actual number of DLCIs you can configure for each channel is determined by the capabilities of your system, such as the number and types of PICs installed. If the number of DLCIs in the configuration exceeds the capabilities of your system, the routing platform might not be able to support the maximum DLCI values shown in Table 22. To determine the capabilities of your system, please contact Juniper Networks customer support.

Table 22: Frame Relay DLCI Limitations for Channelized Interfaces

PIC Types	Number of DLCIs per Level	Range
Original Channelized PICs		
DS0 level channels	3 for sparse mode	1–1022 for sparse mode (0 is reserved for the Local Management Interface [LMI])
T3 and T1 level channels	64 for regular mode 3 for sparse mode	1–63 for regular mode 1–1022 for sparse mode (0 is reserved for the LMI)
Channelized IQ PICs		
DS0 level channels (Channelized DS3 IQ, Channelized STM1 IQ, Channelized E1 IQ, Channelized OC3 IQ, or Channelized OC12 IQ PICs)	16	1–1022 (0 is reserved for the LMI)
E1 level channels (Channelized E1 IQ PIC)	16	1–1022 (0 is reserved for the LMI)
E1 level channels (Channelized STM1 IQ PIC)	64	1–1022 (0 is reserved for the LMI)
OC3 level channels (Channelized OC3 IQ or Channelized OC12 IQ PIC)	64	1–1022 (0 is reserved for the LMI)
OC12 level channels (Channelized OC12 IQ PIC)		
STM1 level channel (Channelized STM1 IQ PIC)	64	1–1022 (0 is reserved for the LMI)
T1 level channels (Channelized DS3 IQ PIC)	16	1–1022 (0 is reserved for the LMI)
T1 level channels (Channelized OC3 IQ or Channelized OC12 IQ PIC)	64	1–1022 (0 is reserved for the LMI)
T3 level channel (Channelized DS3 IQ, Channelized OC3 IQ, or Channelized OC12 IQ PIC)	256	1–1022 (0 is reserved for the LMI)

Clock Sources on Channelized Interfaces

Channelized interfaces and channelized IQ interfaces have different clocking capabilities. For channelized IQ interfaces, you can configure clocking on each port independently by including the clocking (internal | external) statement at the [edit interfaces *interface-name*] hierarchy level.

For channelized IQ interfaces, clocking is provided as follows:

SONET/SDH-level clocking is provided at the [edit interfaces *coc3-fpc/pic/port*], [edit interfaces *coc12-fpc/pic/port*], and [edit interfaces *cstm-1-fpc/pic/port*] hierarchy levels.

T3-level clocking is provided at the [edit interfaces *ct3-fpc/pic/port*] hierarchy level.

T1-level clocking is provided at the [edit interfaces *t1-fpc/pic/port<:channel>*] hierarchy level.

E1-level clocking is provided at the [edit interfaces *ce1-fpc/pic/port*] hierarchy level.

Clocking for all *NxDS0* channels is provided at the [edit interfaces *ct1-fpc/pic/port<:channel>*] or [edit interfaces *ce1-fpc/pic/port*] hierarchy level.

The clocking statement is ignored if you include it at the [edit interfaces *coc1-fpc/pic/port:channel*] or [edit interfaces *cau4-fpc/pic/port:channel*] hierarchy level.

If you include the clocking statement at the channelized and interface levels—*coc12-fpc/pic/port* and *so-fpc/pic/port*, for example—the clocking configuration at the channelized level, *coc12-fpc/pic/port* in this example, takes precedence.

For channelized interfaces, clocking at each channel level is provided as follows:

For channelized OC12, DS3, and E1 interfaces, the clocking statement is supported only for channel 0; it is ignored if included in the configuration of other channels. For channelized STM1 interfaces, the clocking statement is supported only channels 0 through 62.

The clock source configured for channel 0 applies to all channels on the channelized interfaces.

When you configure the clock source for a channelized interface—*t3-pc/pic/port:0*, for example—you must also include the channel-group statement at the [edit chassis] hierarchy level, and specify channel group 0.

For channelized T3 interfaces, you can configure external clocking (loop timing) on all T1 channels under the channelized T3 interface. The loop-timing and no-loop-timing statements apply only to channelized T3 interfaces. If you attempt to include these statements on any other interface type, they are ignored. To configure loop timing for all T1 channels under the channelized T3 interface, include the loop-timing statement at the [edit interfaces ct3-fpc/pic/port t3-options] hierarchy level.

For channelized STM1 interfaces, you should configure the clock source at one side of the connection to be internal and configure the other side of the connection to be external.

Table 23 lists the clocking capabilities for each channelized PIC.

Table 23: Clocking Capabilities by Channelized PIC Type

PIC Type	SONET/SDH Level	DS3 Level	DS1/E1 Level
Channelized PICs			
Channelized DS3 and Multichannel DS3	Not applicable.	The loop-timing statement is supported at the [edit interfaces t1-fpc/pic/port:0 t3-options] or [edit interfaces ds-fpc/pic/port:0:0 t3-options] hierarchy level.	The clocking statement is supported at the [edit interfaces t1-fpc/pic/port:0] or [edit interfaces ds-fpc/pic/port:0:0] hierarchy level.
Channelized E1	Not applicable.	Not applicable.	The clocking statement is supported at the [edit interfaces e1-fpc/pic/port:0] or [edit interfaces ds-fpc/pic/port:0] hierarchy level.
Channelized OC12	Not configurable.	The clocking statement is supported at the [edit interfaces t3-fpc/pic/port:0] hierarchy level.	Not applicable.
Channelized STM1	Not configurable.	Not applicable.	The clocking statement is supported at the [edit interfaces e1-fpc/pic/port:[0-62]] hierarchy level.
Channelized IQ PICs			
Channelized DS3 IQ	Not applicable.	The clocking statement is supported at the [edit interfaces ct3-fpc/pic/port] hierarchy level. The clocking statement is ignored if you include it at the [edit interfaces t3-fpc/pic/port] hierarchy level.	For T1 channels, the clocking statement is supported at the [edit interfaces t1-fpc/pic/port:[1-28]] hierarchy level. For NxDS0 channels, the clocking statement is supported at the [edit interfaces ct1-fpc/pic/port:[1-28]] hierarchy level.
Channelized E1 IQ	Not applicable.	Not applicable.	For E1 and NxDS0 channels, the clocking statement is supported at the [edit interfaces ce1-fpc/pic/port] hierarchy level. The clocking statement is ignored if you include it at the [edit interfaces e1-fpc/pic/port] hierarchy level.

PIC Type	SONET/SDH Level	DS3 Level	DS1/E1 Level
Channelized OC3 IQ	The clocking statement is supported at the [edit interfaces <i>coc3-fpc/pic/port</i>] hierarchy level. The clocking statement is ignored if you include it at the [edit interfaces <i>so-fpc/pic/port</i>] hierarchy level.	The clocking statement is supported at the [edit interfaces <i>t3-fpc/pic/port:[1-12]</i>] hierarchy level. The clocking statement is ignored if you include it at the [edit interfaces <i>coc1-fpc/pic/port:channel</i>] hierarchy level.	The clocking statement is supported at the [edit interfaces <i>ct1-fpc/pic/port:[1-12]:[1-28]</i>] and [edit interfaces <i>t1-fpc/pic/port:[1-12]:[1-28]</i>] hierarchy levels.
Channelized OC12 IQ	The clocking statement is supported at the [edit interfaces <i>coc12-fpc/pic/port</i>] hierarchy level. The clocking statement is ignored if you include it at the [edit interfaces <i>so-fpc/pic/port</i>] hierarchy level.	The clocking statement is supported at the [edit interfaces <i>t3-fpc/pic/port:[1-12]</i>] hierarchy level. The clocking statement is ignored if you include it at the [edit interfaces <i>coc1-fpc/pic/port:channel</i>] hierarchy level.	The clocking statement is supported at the [edit interfaces <i>ct1-fpc/pic/port:[1-12]:[1-28]</i>] and [edit interfaces <i>t1-fpc/pic/port:[1-12]:[1-28]</i>] hierarchy levels.
Channelized STM1 IQ	The clocking statement is supported at the [edit interfaces <i>cstm-1-fpc/pic/port</i>] hierarchy level. The clocking statement is ignored if you include it at the [edit interfaces <i>cau4-fpc/pic/port:channel</i>] or [edit interfaces <i>so-fpc/pic/port</i>] hierarchy level.	Not applicable.	For E1 and NxDS0 channels, the clocking statement is supported at the [edit interfaces <i>ce1-fpc/pic/port[1-63]</i>] hierarchy level. The clocking statement is ignored if you include it at the [edit interfaces <i>e1-fpc/pic/port</i>] hierarchy level.

Channelized IQ Interface Properties

On channelized IQ interfaces, you can specify options that are globally applied to all interface types associated with a channelized IQ interface. For example, e1-options statements that you include at the [edit interfaces *ce1-fpc/pic/port*] hierarchy level apply globally to all E1 and NxDS0 interfaces that you create by partitioning *ce1-fpc/pic/port*. Likewise, t3-options statements that you include at the [edit interfaces *ct3-fpc/pic/port*] hierarchy level apply globally to all T1 and NxDS0 interfaces that you create by partitioning *ct3-fpc/pic/port*.

You can also apply interface options at the channel level. For example, you can include t1-options statements at the [edit interfaces *t1-fpc/pic/port<:channel>*] hierarchy level, and ds0-options statements at the [edit interfaces *ds-0/1/1<:channel>*] hierarchy level.

Only a subset of the interface options is valid on each type of channelized IQ interface. You configure all HDLC information at the end data channel level, not at the parent level. For example, you configure HDLC information at the [edit interfaces *ds-fpc/pic/port<:channel>*] hierarchy level, not at the [edit interfaces *ct1-fpc/pic/port<:channel>*] hierarchy level.

Channelized IQ interfaces do not support receive buckets or transmit buckets.

For channelized IQ interfaces, there are some limitations on where you place certain statements in the configuration. When you configure clocking, bit error rate testing (BERT), C-bit parity, and loopback statements on T3, T1, or DS0 channels, you must follow these guidelines:

For T3 IQ interfaces, you can include the loopback payload statement at the [edit interfaces ct3-*fpc/pic/port*] and [edit interfaces t3-*fpc/pic/port:channel*] hierarchy levels. For T1 interfaces, you can include the loopback payload statement in the configuration at the [edit interfaces t1-*fpc/pic/port:channel*] hierarchy level; it is ignored if included at the [edit interfaces ct1-*fpc/pic/port*] hierarchy level. For NxDS0 interfaces, payload and remote loopback are the same. If you configure one, the other is ignored. NxDS0 IQ interfaces do not support local loopback.

If you include clocking, BERT, and C-bit parity configurations at both the [edit interfaces ct3-*fpc/pic/port<:channel>* t3-options] and [edit interfaces t3-*fpc/pic/port<:channel>* t3-options] hierarchy levels, the channelized T3-level statements are valid, and the T3-level statements are ignored.

If you include clocking, BERT, and C-bit parity configurations at both the [edit interfaces ct3-*fpc/pic/port<:channel>* t3-options] and [edit interfaces t1-*fpc/pic/port<:channel>* t1-options] hierarchy levels, the channelized T3-level statements are operational for the T3 connections and the T1-level statements are operational for the T1 connections.

Because DS0 channels do not have clocking capability, you must configure clocking at the [edit interfaces ct1-*fpc/pic/port<:channel>* t1-options] or [edit interfaces ce1-*fpc/pic/port<:channel>* e1-options] hierarchy level for channelized NxDS0 IQ interfaces.

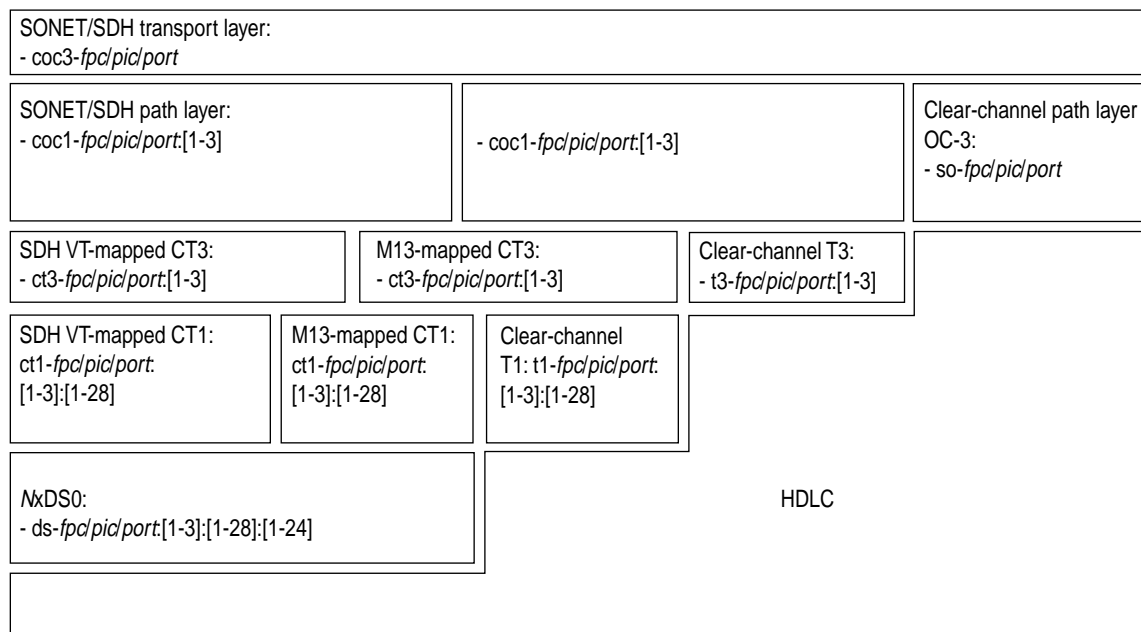
You can set BERT at the [edit interfaces t3-*fpc/pic/port<:channel>* t3-options] hierarchy level or on any partitioned channel of the channelized T3 interface. There are twelve BERT patterns available for NxDS0 channels and twenty-eight BERT patterns for T1, channelized T1, T3, and channelized T3 interfaces within channelized IQ interfaces.

For channelized interfaces that use Frame Relay encapsulation, the number of configurable DLCIs varies by channelized interface type.

Structure of Channelized IQ PICs

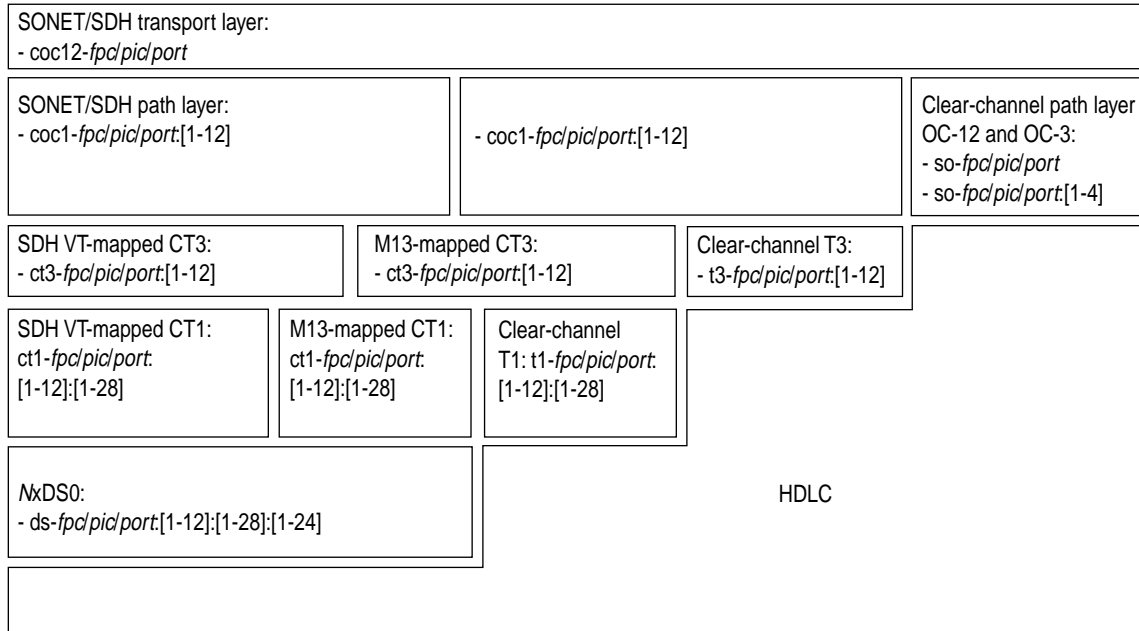
Figure 12, Figure 13 on page 255, Figure 14 on page 255, Figure 15 on page 256, and Figure 16 on page 256 show the structural organization of the Channelized OC3 IQ PIC, Channelized OC12 IQ PIC, Channelized STM1 IQ PIC, Channelized DS3 IQ PIC, and Channelized E1 IQ PIC. Table 24 on page 256 shows the structure of all channelized PICs, including channelized IQ PICs and channelized PICs.

Figure 12: Structure of the Channelized OC3 IQ PIC



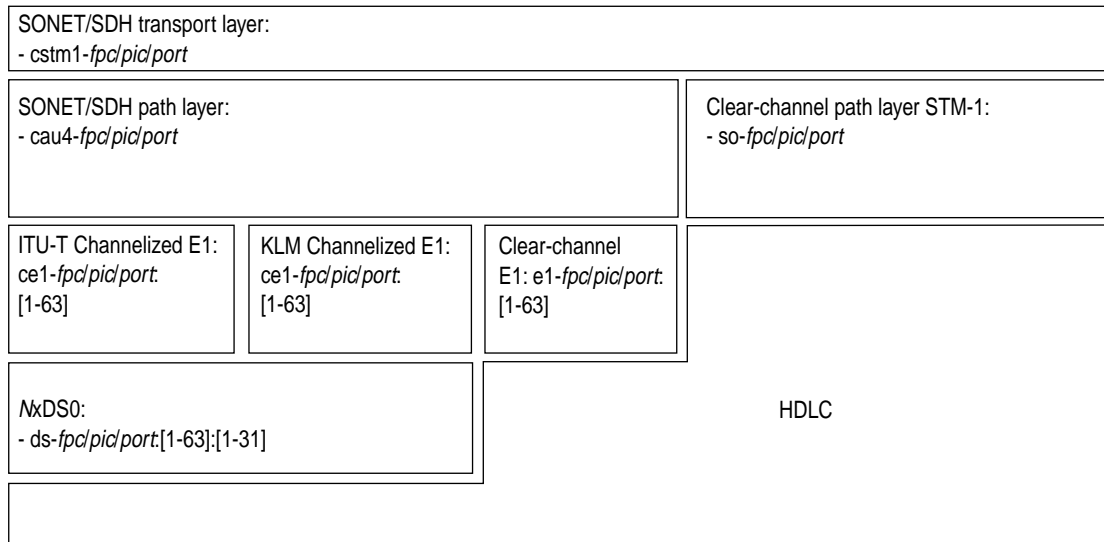
9015502

Figure 13: Structure of the Channelized OC12 IQ PIC



g003012

Figure 14: Structure of the Channelized STM1 IQ PIC



g003087

Figure 15: Structure of the Channelized DS3 IQ PIC

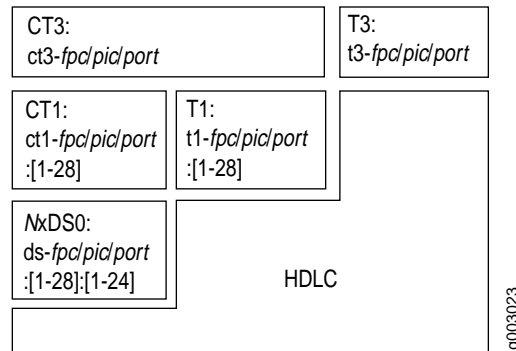


Figure 16: Structure of the Channelized E1 IQ PIC

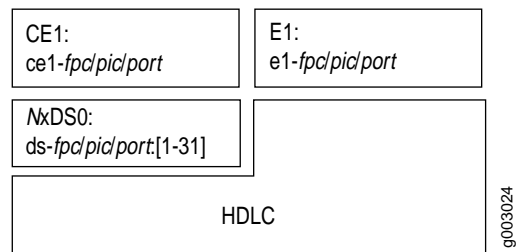


Table 24: Structural Differences: Channelized PICs and Channelized IQ PICs

PIC Type	Transport	Path	DS3	DS1/E1
Channelized PICs				
Channelized E1	Not applicable.	Not applicable.	Not applicable.	e1-fpc/pic/port ds-fpc/pic/port:0
Channelized OC12	t3-fpc/pic/port:0	t3-fpc/pic/port:[0-11]	t3-fpc/pic/port:[0-11]	Not applicable.
Channelized STM1	e1-fpc/pic/port:0	e1-fpc/pic/port:0	Not applicable.	e1-fpc/pic/port:[0-63]
Channelized T3 and Multichannel T3	Not applicable.	Not applicable.	t1-fpc/pic/port:0	t1-fpc/pic/port:[0-27]
Channelized IQ PICs				
Channelized IQ DS3	Not applicable.	Not applicable.	ct3-fpc/pic/port t3-fpc/pic/port	ct1-fpc/pic/port:[1-28] t1-fpc/pic/port:[1-28]
Channelized IQ E1	Not applicable.	Not applicable.	Not applicable.	ce1-fpc/pic/port e1-fpc/pic/port
Channelized IQ OC3	coc3-fpc/pic/port	coc1-fpc/pic/port:[1-3] so-fpc/pic/port	ct3-fpc/pic/port:[1-3] t3-fpc/pic/port:[1-3]	ct1-fpc/pic/port:[1-3]:[1-28] t1-fpc/pic/port:[1-3]:[1-28]
Channelized IQ OC12	coc12-fpc/pic/port	coc1-fpc/pic/port:[1-12] so-fpc/pic/port	ct3-fpc/pic/port:[1-12] t3-fpc/pic/port:[1-12]	ct1-fpc/pic/port:[1-3]:[1-28] t1-fpc/pic/port:[1-3]:[1-28]
Channelized IQ STM1	Not applicable.	cau4-fpc/pic/port so-fpc/pic/port	Not applicable.	ce1-fpc/pic/port:[1-63] e1-fpc/pic/port:[1-63]