

Chapter 12

Channelized Interfaces Overview

Channelized interfaces enable you to configure a number of individual channels that subdivide the bandwidth of a larger interface and minimize the number of PICs that an installation requires.



NOTE: Channelized intelligent queuing (IQ) interfaces require M-series Enhanced FPCs.

Wherever the *JUNOS Internet Software Configuration Guides* refer to channelized interfaces and PICs without the “intelligent queuing” or “IQ” descriptor, they are referring to the original channelized interfaces and PICs.

For channelized IQ logical interfaces, you can configure class of service (CoS). For more information, see “Configure Logical Interface Scheduling” on page 783.

This chapter provides a high-level overview of channelized interfaces, focusing mainly on the capabilities, properties, and structure of channelized IQ interfaces:

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Channelized Interface Capabilities

You can configure each port of a channelized IQ PIC as a single interface that uses the entire available bandwidth, or partition each port into smaller data channels. Following are the interface names associated with channelized IQ PICs:

coc12-fpc/pic/port—On a Channelized OC-12 IQ PIC

coc1-fpc/pic/port:channel—On a Channelized OC-12 IQ PIC

ct3-fpc/pic/port<:channel>—On a Channelized OC-12 IQ or Channelized DS-3 IQ PIC

cstm1-fpc/pic/port—On a Channelized STM-1 IQ PIC

cau4-fpc/pic/port:channel—On a Channelized STM-1 IQ PIC

ct1-fpc/pic/port<:channel>—On a Channelized OC-12 IQ or Channelized DS-3 IQ PIC

ce1-fpc/pic/port<:channel>—On a Channelized E1 IQ or a Channelized STM-1 IQ PIC

E1 channels—*e1-fpc/pic/port<:channel>*, configure on a Channelized E1 IQ or a Channelized STM-1 IQ PIC

NxDS-0 channels—*ds-fpc/pic/port<:channel>*, configure on a Channelized OC-12 IQ, Channelized STM-1 IQ, Channelized DS-3 IQ, or Channelized E1 IQ PIC

SONET/SDH channels—*so-fpc/pic/port:channel*, configure four OC-3 channels on a Channelized OC-12 IQ PIC, one OC-12 channel on a Channelized OC-12 IQ PIC, or one STM-1 channel on a Channelized STM-1 IQ PIC

T1 channels—*t1-fpc/pic/port<:channel>*, configure on a Channelized OC-12 IQ or Channelized DS-3 IQ PIC

T3 channels—*t3-fpc/pic/port<:channel>*, configure on a Channelized OC-12 IQ or Channelized DS-3 IQ PIC

Data-Link Connection Identifiers on Channelized Interfaces

If you use Frame Relay encapsulation on a channelized interface, see Table 17 for the maximum number of data-link connection identifiers (DLCIs) per channel that you can configure at each channel level for various channelized PICs.



NOTE: The actual number of DLCIs you can configure for each channel is determined by the capabilities of your system, such as the number and types of PICs installed. If the number of DLCIs in the configuration exceeds the capabilities of your system, the routing platform might not be able to support the maximum DLCI values shown in Table 17. To determine the capabilities of your system, please contact Juniper Networks customer support.

Table 17: Frame Relay DLCI Limitations for Channelized Interfaces

Original Channelized PICs	Number of DLCIs per level	Range
T3 and T1 level channels	64 for regular mode 3 for sparse mode	0—64 for regular mode 1—1022 for sparse mode (0 is reserved for the Local Management Interface or LMI)
DS-0 level channels	3 for sparse mode	1—1022 for sparse mode (0 is reserved for LMI)
Channelized IQ PICs	Number of DLCIs per level	Range
OC-12 and OC-3 level channels (Channelized OC-12 IQ PIC)	64	1—1022 (0 is reserved for LMI)
T3 level channel (Channelized OC-12 IQ PIC)	256	1—1022 (0 is reserved for LMI)
T3 level channel (Channelized DS-3 IQ PIC)	256	1—1022 (0 is reserved for LMI)
STM-1 level channel (Channelized STM-1 IQ PIC)	64	1—1022 (0 is reserved for LMI)
E1 level channels (Channelized STM-1 IQ PIC)	64	1—1022 (0 is reserved for LMI)
E1 level channels (Channelized E1 IQ PIC)	16	1—1022 (0 is reserved for LMI)
T1 level channels (Channelized OC-12 IQ PIC)	64	1—1022 (0 is reserved for LMI)
T1 level channels (Channelized DS-3 IQ PIC)	16	1—1022 (0 is reserved for LMI)
DS-0 level channels (Channelized DS-3 IQ, Channelized STM-1 IQ, Channelized E1 IQ, or Channelized OC-12 IQ PICs)	16	1—1022 (0 is reserved for LMI)

Clock Sources on Channelized Interfaces

Channelized interfaces and channelized IQ interfaces have different clocking capabilities. For channelized IQ interfaces, you can configure clocking on each port independently by including the clocking (internal | external) statement at the [edit interfaces *interface-name*] hierarchy level.

For channelized IQ interfaces, clocking is provided as follows:

SONET/SDH-level clocking is provided at the [edit interfaces *coc12-fpc/pic/port*] and [edit interfaces *cstm1-fpc/pic/port*] hierarchy levels.

T3-level clocking is provided at the [edit interfaces *ct3-fpc/pic/port*] hierarchy level.

T1-level clocking is provided at the [edit interfaces *t1-fpc/pic/port<:channel>*] hierarchy level.

E1-level clocking is provided at the [edit interfaces *ce1-fpc/pic/port*] hierarchy level.

Clocking for all *NxDS-0* channels is provided at the [edit interfaces *ct1-fpc/pic/port<:channel>*] or [edit interfaces *ce1-fpc/pic/port*] hierarchy level.

The clocking statement is ignored if you include it at the [edit interfaces *coc1-fpc/pic/port:channel*] or [edit interfaces *cau4-fpc/pic/port:channel*] hierarchy level.

If you include the clocking statement at the channelized and interface levels—*coc12-fpc/pic/port* and *so-fpc/pic/port*, for example—the clocking configuration at the channelized level, *coc12-fpc/pic/port* in this example, takes precedence.

For channelized interfaces, clocking at each channel level is provided as follows:

For channelized OC-12, DS-3, and E1 interfaces, the clocking statement is supported only for channel 0; it is ignored if included in the configuration of other channels. For channelized STM-1 interfaces, the clocking statement is supported only channels 0 through 62.

The clock source configured for channel 0 applies to all channels on the channelized interfaces.

When you configure the clock source for a channelized interface—`t3-pc/pic/port:0`, for example—you must also include the `channel-group` statement at the [edit chassis] hierarchy level, and specify channel group 0.

For channelized T3 interfaces, you can configure external clocking (loop timing) on all T1 channels under the channelized T3 interface. The `loop-timing` and `no-loop-timing` statements apply only to channelized T3 interfaces. If you attempt to include these statements on any other interface type, they are ignored. To configure loop timing for all T1 channels under the channelized T3 interface, include the `loop-timing` statement at the [edit interfaces `ct3-fpc/pic/port t3-options`] hierarchy level.

For channelized STM-1 interfaces, you should configure the clock source at one side of the connection to be internal and configure the other side of the connection to be external.

Table 18 lists the clocking capabilities for each channelized PIC.

Table 18: Clocking Capabilities by Channelized PIC Type

PIC Type	SONET/SDH Level	DS-3 Level	DS-1/E1 Level
Channelized PICs			
Channelized OC-12	Not configurable.	The clocking statement is supported at the [edit interfaces <code>t3-fpc/pic/port:0</code>] hierarchy level.	Not applicable.
Channelized DS-3 and Multichannel DS-3	Not applicable.	The loop-timing statement is supported at the [edit interfaces <code>t1-fpc/pic/port:0 t3-options</code>] or [edit interfaces <code>ds-fpc/pic/port:0:0 t3-options</code>] hierarchy level.	The clocking statement is supported at the [edit interfaces <code>t1-fpc/pic/port:0</code>] or [edit interfaces <code>ds-fpc/pic/port:0:0</code>] hierarchy level.
Channelized STM-1	Not configurable.	Not applicable.	The clocking statement is supported at the [edit interfaces <code>e1-fpc/pic/port:[0-62]</code>] hierarchy level.
Channelized E1	Not applicable.	Not applicable.	The clocking statement is supported at the [edit interfaces <code>e1-fpc/pic/port:0</code>] or [edit interfaces <code>ds-fpc/pic/port:0</code>] hierarchy level.

PIC Type	SONET/SDH Level	DS-3 Level	DS-1/E1 Level
Channelized IQ PICs			
Channelized OC-12 IQ	<p>The clocking statement is supported at the [edit interfaces coc12-fpc/pic/port].</p> <p>The clocking statement is ignored if you include it at the [edit interfaces so-fpc/pic/port] hierarchy level.</p>	<p>The clocking statement is supported at the [edit interfaces t3-fpc/pic/port:[1-12]] hierarchy level.</p> <p>The clocking statement is ignored if you include it at the [edit interfaces coc1-fpc/pic/port:channel] hierarchy level.</p>	<p>The clocking statement is supported at the [edit interfaces ct1-fpc/pic/port:[1-12]:[1-28]] and [edit interfaces t1-fpc/pic/port:[1-12]:[1-28]] hierarchy levels.</p>
Channelized STM-1 IQ	<p>The clocking statement is supported at the [edit interfaces cstm1-fpc/pic/port] hierarchy level.</p> <p>The clocking statement is ignored if you include it at the [edit interfaces cau4-fpc/pic/port:channel] or [edit interfaces so-fpc/pic/port] hierarchy levels.</p>	Not applicable.	<p>For E1 and NxDS-0 channels, the clocking statement is supported at the [edit interfaces ce1-fpc/pic/port{1-63}].</p> <p>The clocking statement is ignored if you include it at the [edit interfaces e1-fpc/pic/port] hierarchy level.</p>
Channelized DS-3 IQ	Not applicable.	<p>The clocking statement is supported at the [edit interfaces ct3-fpc/pic/port].</p> <p>The clocking statement is ignored if you include it at the [edit interfaces t3-fpc/pic/port] hierarchy level.</p>	<p>For T1 channels, the clocking statement is supported at the [edit interfaces t1-fpc/pic/port:[1-28]] hierarchy level.</p> <p>For NxDS-0 channels, the clocking statement is supported at the [edit interfaces ct1-fpc/pic/port:[1-28]] hierarchy level.</p>
Channelized E1 IQ	Not applicable.	Not applicable.	<p>For E1 and NxDS-0 channels, the clocking statement is supported at the [edit interfaces ce1-fpc/pic/port].</p> <p>The clocking statement is ignored if you include it at the [edit interfaces e1-fpc/pic/port] hierarchy level.</p>

Channelized IQ Interface Properties

On channelized IQ interfaces, you can specify options that are globally applied to all interface types associated with a channelized IQ interface. For example, e1-options statements that you include at the [edit interfaces ce1-*fpc/pic/port*] hierarchy level apply globally to all E1 and NxDS-0 interfaces that you create by partitioning ce1-*fpc/pic/port*. Likewise, t3-options statements that you include at the [edit interfaces ct3-*fpc/pic/port*] hierarchy level apply globally to all T1 and NxDS-0 interfaces that you create by partitioning ct3-*fpc/pic/port*.

You can also apply interface options at the channel level. For example, you can include t1-options statements at the [edit interfaces t1-*fpc/pic/port*<:*channel*>] hierarchy level, and ds0-options statements at the [edit interfaces ds-0/1/1<:*channel*>] hierarchy level.

Only a subset of the interface options is valid on each type of channelized IQ interface. You configure all HDLC information at the end data channel level, not at the parent level. For example, you configure HDLC information at the [edit interfaces ds-*fpc/pic/port*<:*channel*>] hierarchy level, not at the [edit interfaces ct1-*fpc/pic/port*<:*channel*>] hierarchy level.

Channelized IQ interfaces do not support receive buckets or transmit buckets.

For channelized IQ interfaces, there are some limitations on where you place certain statements in the configuration. When you configure clocking, bit error rate testing (BERT), C-bit parity, and loopback statements on T3, T1, or DS-0 channels, you must follow these guidelines:

For T3 IQ interfaces, you can include the loopback payload statement at the [edit interfaces ct3-*fpc/pic/port*] and [edit interfaces t3-*fpc/pic/port:channel*] hierarchy levels. For T1 interfaces, you can include the loopback payload statement in the configuration at the [edit interfaces t1-*fpc/pic/port:channel*] hierarchy level; it is ignored if included at the [edit interfaces ct1-*fpc/pic/port*] hierarchy level. For NxDS-0 interfaces, payload and remote loopback are the same. If you configure one, the other is ignored. NxDS-0 IQ interfaces do not support local loopback.

If you include clocking, BERT, and C-bit parity configurations at both the [edit interfaces ct3-*fpc/pic/port*<:*channel*> t3-options] and [edit interfaces t3-*fpc/pic/port*<:*channel*> t3-options] hierarchy levels, the channelized T3-level statements are valid, and the T3-level statements are ignored.

If you include clocking, BERT, and C-bit parity configurations at both the [edit interfaces ct3-*fpc/pic/port*<:*channel*> t3-options] and [edit interfaces t1-*fpc/pic/port*<:*channel*> t1-options] hierarchy levels, the channelized T3-level statements are operational for the T3 connections and the T1-level statements are operational for the T1 connections.

Because DS-0 channels do not have clocking capability, you must configure clocking at the [edit interfaces ct1-*fpc/pic/port*<:*channel*> t1-options] or [edit interfaces ce1-*fpc/pic/port*<:*channel*> e1-options] hierarchy level for channelized NxDS-0 IQ interfaces.

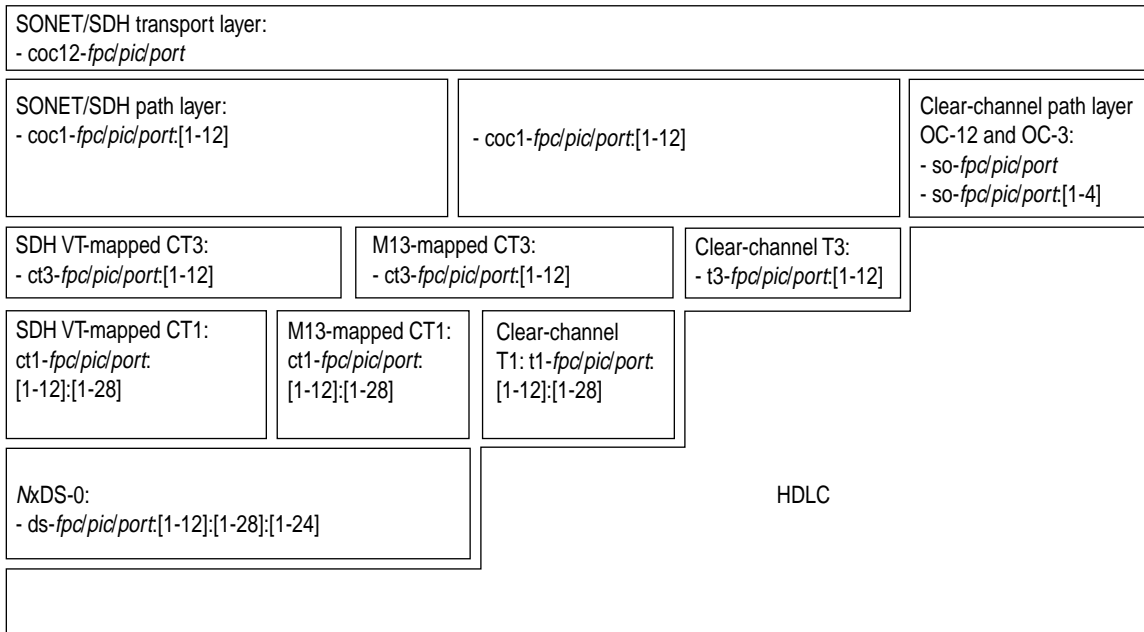
You can set BERT at the [edit interfaces t3-fpc/pic/port<:channel> t3-options] hierarchy level or on any partitioned channel of the channelized T3 interface. There are twelve BERT patterns available for NxDS-0 channels and twenty-eight BERT patterns for T1, channelized T1, T3, and channelized T3 interfaces within channelized IQ interfaces.

For channelized interfaces that use Frame Relay encapsulation, the number of configurable data-link connection identifiers (DLCIs) varies by channelized interface type.

Structure of Channelized IQ PICs

Figure 11, Figure 12, Figure 13, and Figure 14 show the structural organization of the Channelized OC-12 IQ PIC, Channelized STM-1 IQ PIC, Channelized DS-3 IQ PIC, and Channelized E1 IQ PIC. Table 19 on page 232 shows the structure of all channelized PICs, including channelized IQ PICs and channelized PICs.

Figure 11: Structure of the Channelized OC-12 IQ PIC



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Figure 12: Structure of the Channelized STM-1 IQ PIC

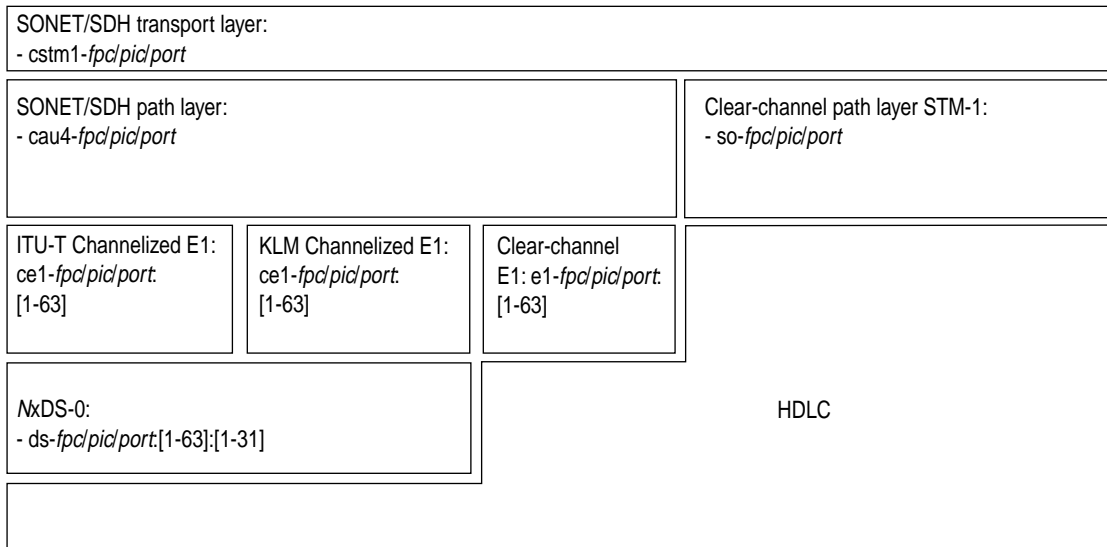


Figure 13: Structure of the Channelized DS-3 IQ PIC

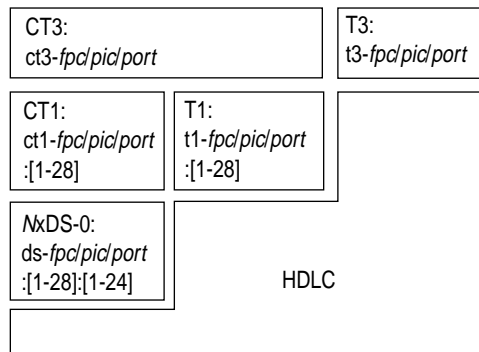


Figure 14: Structure of the Channelized E1 IQ PIC

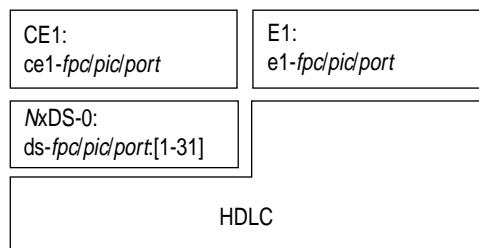


Table 19: Structural Differences: Channelized PICs and Channelized IQ PICs

PIC Type	Transport	Path	DS-3	DS-1/E1
Channelized PICs				
Channelized OC-12	<i>t3-fpc/pic/port:0</i>	<i>t3-fpc/pic/port:[0-11]</i>	<i>t3-fpc/pic/port:[0-11]</i>	Not applicable.
Channelized T3 and Multichannel T3	Not applicable.	Not applicable.	<i>t1-fpc/pic/port:0</i>	<i>t1-fpc/pic/port:[0-27]</i>
Channelized STM-1	<i>e1-fpc/pic/port:0</i>	<i>e1-fpc/pic/port:0</i>	Not applicable.	<i>e1-fpc/pic/port:[0-63]</i>
Channelized E1	Not applicable.	Not applicable.	Not applicable.	<i>e1-fpc/pic/port</i> <i>ds-fpc/pic/port:0</i>
Channelized IQ PICs				
Channelized IQ OC-12	<i>coc12-fpc/pic/port</i>	<i>coc1-fpc/pic/port:[1-12]</i> <i>so-fpc/pic/port</i>	<i>ct3-fpc/pic/port:[1-12]</i> <i>t3-fpc/pic/port:[1-12]</i>	<i>ct1-fpc/pic/port:[1-12]:[1-28]</i> <i>t1-fpc/pic/port:[1-12]:[1-28]</i>
Channelized IQ STM-1	Not applicable.	<i>cau4-fpc/pic/port</i> <i>so-fpc/pic/port</i>	Not applicable.	<i>ce1-fpc/pic/port:[1-63]</i> <i>e1-fpc/pic/port:[1-63]</i>
Channelized IQ DS-3	Not applicable.	Not applicable.	<i>ct3-fpc/pic/port</i> <i>t3-fpc/pic/port</i>	<i>ct1-fpc/pic/port:[1-28]</i> <i>t1-fpc/pic/port:[1-28]</i>
Channelized IQ E1	Not applicable.	Not applicable.	Not applicable.	<i>ce1-fpc/pic/port</i> <i>e1-fpc/pic/port</i>