

Chapter 12

Channelized Interfaces Overview

Channelized interfaces enable you to configure a number of individual channels that subdivide the bandwidth of a larger interface and minimize the number of PICs that an installation requires.



Note

Channelized QPP interfaces require M-series Enhanced FPCs.

Wherever the *JUNOS Internet Software Configuration Guides* refer to channelized interfaces and PICs without the “Q Performance Processor” or “QPP” descriptor, they are referring to the original channelized interfaces and PICs.

For channelized QPP logical interfaces, you can configure class of service (CoS). For more information, see “Associate a Scheduler with a DLCI or VLAN on a Channelized QPP Interface” on page 597.

This chapter provides a high-level overview of channelized interfaces, focusing mainly on the capabilities, properties, and structure of channelized QPP interfaces:

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Channelized Interface Capabilities

You can configure each port of a Channelized PIC with QPP as a single interface that uses the entire available bandwidth, or partition each port into smaller data channels. Following are the interface names associated with Channelized PICs with QPP:

coc12-fpc/pic/port—On a Channelized OC-12 PIC

coc1-fpc/pic/port:channel—On a Channelized OC-12 PIC

ct3-fpc/pic/port<:channel>—On a Channelized OC-12 or Channelized DS-3 PIC

cstm1-fpc/pic/port—On a Channelized STM-1 PIC

cau4-fpc/pic/port:channel—On a Channelized STM-1 PIC

ct1-fpc/pic/port<:channel>—On a Channelized OC-12 or Channelized DS-3 PIC

ce1-fpc/pic/port<:channel>—On a Channelized E1 or a Channelized STM-1 PIC

so-fpc/pic/port—One OC-12 channel on a Channelized OC-12 PIC or one STM-1 channel on a Channelized STM-1 PIC

t3-fpc/pic/port<:channel>—On a Channelized OC-12 or Channelized DS-3 PIC

e1-fpc/pic/port<:channel>—On a Channelized E1 a Channelized STM-1 PIC

so-fpc/pic/port:channel—Four OC3 channels on a Channelized OC-12 PIC

t1-fpc/pic/port<:channel>—On a Channelized OC-12 or Channelized DS-3 PIC

ds-fpc/pic/port<:channel>—On a Channelized OC-12, Channelized STM-1, Channelized DS-3, or Channelized E1 PIC

Table 14 lists the number of supported interfaces on Channelized PICs with QPP.

Table 14: Supported Interfaces on Channelized PICs with QPP

Interface Types	1-Port Channelized OC-12 PIC with QPP	1-port Channelized STM-1 PIC with QPP	4-Port Channelized DS-3 PIC with QPP	10-Port Channelized E1 PIC with QPP
OC-12 interfaces	1	None	None	None
OC-3 interfaces	4	None	None	None
STM-1 interfaces	None	1	None	None
T3 interfaces	12	None	4	None
T1 interfaces	336	None	112	None
E1 interfaces	None	63	None	10
NxDS-0 interfaces	336	128	128—If the “N” in NxDS-0 is 8 or less. 256—If the “N” in NxDS-0 is 9 or more.	310
	Maximum interfaces supported: 336	Maximum interfaces supported: 128	Maximum interfaces supported: 256	Maximum interfaces supported: 310

Following are the interfaces that you can configure on the Channelized PICs:

T3 channels—`t3-fpc/pic/port<:channel>` (on an Channelized OC-12 PIC)

E1 channels—`e1-fpc/pic/port` (on a Channelized E1 or STM-1 PIC)

T1 channels—`t1-fpc/pic/port<:channel>` (on a Channelized DS-3 PIC)

NxDS-0 channels—`ds-fpc/pic/port<:channel>` (on a Channelized DS-3 or Channelized E1 PIC)

Data Link Connection Identifiers on Channelized Interfaces

Table 15 shows the DLCIs that you can configure at each channel level.

Table 15: Frame Relay DLCI Limitations for Channelized Interfaces

Channelized PICs	Number of DLCIs per level	Range
Channelized DS-3	64 in regular mode	0 through 64 for regular mode
Channelized STM-1	3 in sparse mode	0 through 1022 for sparse mode (0 is reserved for LMI)
Multichannel DS-3	3	0 through 1022
Channelized E1		
Channelized PICs with QPP	Number of DLCIs per level	Range
Channelized OC-12	64 for T3, OC-3, SONET, and Channelized OC-12 interfaces 16 for T1 and NxDS-0 interfaces	0 through 1022 for sparse mode (0 is reserved for LMI)
Channelized STM-1	64 for SONET interfaces 16 for E1 and NxDS-0 interfaces	0 through 1022 for sparse mode (0 is reserved for LMI)
Channelized DS-3	64 for T3 interfaces 16 for T1 and NxDS-0 interfaces	0 through 1022 for sparse mode (0 is reserved for LMI)
Channelized E1	16	0 through 1022 for sparse mode (0 is reserved for LMI)

Clock Sources on Channelized Interfaces

Channelized interfaces and channelized QPP interfaces have different clocking capabilities. For channelized QPP interfaces, you can configure clocking on each port independently by including the clocking (internal | external) statement at the [edit interfaces *interface-name*] hierarchy level.

For channelized QPP interfaces, clocking is provided as follows:

SONET-level clocking is provided at the [edit interfaces *coc12-fpc/pic/port*] and [edit interfaces *cstm1-fpc/pic/port*] hierarchy levels.

T3-level clocking is provided at the [edit interfaces *ct3-fpc/pic/port*] hierarchy level.

T1-level clocking is provided at the [edit interfaces *t1-fpc/pic/port<:channel>*] hierarchy level.

E1-level clocking is provided at the [edit interfaces *ce1-fpc/pic/port*] hierarchy level.

Clocking for all NxDS-0 channels is provided at the [edit interfaces *ct1-fpc/pic/port<:channel>*] or [edit interfaces *ce1-fpc/pic/port*] hierarchy level.

The clocking statement is ignored if you include it at the [edit interfaces *coc1-fpc/pic/port:channel*] or [edit interfaces *cau4-fpc/pic/port:channel*] hierarchy level.

If you include the clocking statement at the channelized and interface levels—*coc12-fpc/pic/port* and *so-fpc/pic/port*, for example—the clocking configuration at the channelized level, *coc12-fpc/pic/port* in this example, takes precedence.

For channelized interfaces, clocking at each channel level is provided as follows:

The clocking statement is supported only for channel 0; it is ignored if included in the configuration of other channels.

The clock source configured for channel 0 applies to all channels on the channelized interfaces.

When you configure the clock source for a channelized interface—`t3-pc/pic/port:0`, for example—you must also include the `channel-group` statement at the [edit chassis] hierarchy level, and specify channel group 0.

For Channelized T3 interfaces, you can configure external clocking (loop timing) on all T1 channels under the Channelized T3 interface. The `loop-timing` and `no-loop-timing` statements apply only to Channelized T3 interfaces. If you attempt to configure these statements on any other interface type, they are ignored. To configure loop timing for all T1 channels under the Channelized T3 interface, include the `loop-timing` statement at the [edit interfaces `ct3-fpc/pic/port t3-options`] hierarchy level.

For Channelized STM-1 interfaces, you should configure the clock source at one side of the connection to be internal and configure the other side of the connection to be external.

Table 16 lists the clocking capabilities for each channelized PIC.

Table 16: Clocking Capabilities by Channelized PIC Type

PIC Type	SONET Level	DS-3 Level	DS-1/E1 Level
Channelized PICs			
Channelized OC-12	Not configurable.	The clocking statement is supported at the [edit interfaces <code>t3-fpc/pic/port:0</code>] hierarchy level.	Not applicable.
Channelized DS-3 and Multichannel DS-3	Not applicable.	The loop-timing statement is supported at the [edit interfaces <code>t1-fpc/pic/port:0 t3-options</code>] or [edit interfaces <code>ds-fpc/pic/port:0:0 t3-options</code>] hierarchy level.	The clocking statement is supported at the [edit interfaces <code>t1-fpc/pic/port:0</code>] or [edit interfaces <code>ds-fpc/pic/port:0:0</code>] hierarchy level.
Channelized STM-1	Not configurable.	Not applicable.	The clocking statement is supported at the [edit interfaces <code>e1-fpc/pic/port:[0-62]</code>] hierarchy level.
Channelized E1	Not applicable.	Not applicable.	The clocking statement is supported at the [edit interfaces <code>e1-fpc/pic/port:[0-9]</code>] or [edit interfaces <code>ds-fpc/pic/port:0</code>] hierarchy level.
Channelized PICs with QPP			

PIC Type	SONET Level	DS-3 Level	DS-1/E1 Level
Channelized OC-12 with QPP	<p>The clocking statement is supported at the [edit interfaces coc12-<i>fpc/pic/port</i>].</p> <p>The clocking statement is ignored if you include it at the [edit interfaces so-<i>fpc/pic/port</i>] hierarchy level.</p>	<p>The clocking statement is supported at the [edit interfaces t3-<i>fpc/pic/port</i>:<i>[1-12]</i>] hierarchy level.</p> <p>The clocking statement is ignored if you include it at the [edit interfaces coc1-<i>fpc/pic/port:channel</i>] hierarchy level.</p>	<p>The clocking statement is supported at the [edit interfaces ct1-<i>fpc/pic/port</i>:<i>[1-12]</i>:<i>[1-28]</i>] and [edit interfaces t1-<i>fpc/pic/port</i>:<i>[1-12]</i>:<i>[1-28]</i>] hierarchy levels.</p>
Channelized STM-1 with QPP	<p>The clocking statement is supported at the [edit interfaces cstm1-<i>fpc/pic/port</i>] hierarchy level.</p> <p>The clocking statement is ignored if you include it at the [edit interfaces cau4-<i>fpc/pic/port:channel</i>] or [edit interfaces so-<i>fpc/pic/port</i>] hierarchy levels.</p>	Not applicable.	<p>For E1 and NxDS-0 channels, the clocking statement is supported at the [edit interfaces ce1-<i>fpc/pic/port</i><i>[1-63]</i>].</p> <p>The clocking statement is ignored if you include it at the [edit interfaces e1-<i>fpc/pic/port</i>] hierarchy level.</p>
Channelized DS-3 with QPP	Not applicable.	<p>The clocking statement is supported at the [edit interfaces ct3-<i>fpc/pic/port</i>].</p> <p>The clocking statement is ignored if you include it at the [edit interfaces t3-<i>fpc/pic/port</i>] hierarchy level.</p>	<p>For T1 channels, the clocking statement is supported at the [edit interfaces t1-<i>fpc/pic/port</i>:<i>[1-28]</i>] hierarchy level.</p> <p>For NxDS-0 channels, the clocking statement is supported at the [edit interfaces ct1-<i>fpc/pic/port</i>:<i>[1-28]</i>] hierarchy level.</p>
Channelized E1 with QPP	Not applicable.	Not applicable.	<p>For E1 and NxDS-0 channels, the clocking statement is supported at the [edit interfaces ce1-<i>fpc/pic/port</i>].</p> <p>The clocking statement is ignored if you include it at the [edit interfaces e1-<i>fpc/pic/port</i>] hierarchy level.</p>

Channelized QPP Interface Properties

On channelized QPP interfaces, you can specify options that are globally applied to all interface types associated with a channelized QPP interface. For example, e1-options statements that you include at the [edit interfaces ce1-fpc/pic/port] hierarchy level apply globally to all E1 and NxDS-0 interfaces that you create by partitioning ce1-fpc/pic/port. Likewise, t3-options statements that you include at the [edit interfaces ct3-fpc/pic/port] hierarchy level apply globally to all T1 and NxDS-0 interfaces that you create by partitioning ct3-fpc/pic/port.

You can also apply interface options at the channel level. For example, you can include t1-options statements at the [edit interfaces t1-fpc/pic/port<:channel>] hierarchy level, and ds0-options statements at the [edit interfaces ds-0/1/1<:channel>] hierarchy level.

Only a subset of the interface options is valid on each type of channelized QPP interface. You configure all HDLC information at the end data channel level, not at the parent level. For example, you configure HDLC information at the [edit interfaces ds-fpc/pic/port<:channel>] hierarchy level, not at the [edit interfaces ct1-fpc/pic/port<:channel>] hierarchy level.

Channelized QPP interfaces do not support receive buckets or transmit buckets.

There are some limitations for channelized QPP interfaces regarding where you place certain statements in the configuration. When you configure clocking, bit error rate testing (BERT), C-bit parity, and loopback statements on T3, T1, or DS-0 channels, you must follow these guidelines:

For T3 QPP interfaces, you can include the loopback payload statement at the [edit interfaces ct3-fpc/pic/port] and [edit interfaces t3-fpc/pic/port:channel] hierarchy levels. For T1 interfaces, you can include the loopback payload statement in the configuration at the [edit interfaces t1-fpc/pic/port:channel] hierarchy level; it is ignored if included at the [edit interfaces ct1-fpc/pic/port] hierarchy level. For NxDS-0 interfaces, payload and remote loopback are the same. If you configure one, the other is ignored. NxDS-0 QPP interfaces do not support local loopback.

If you include clocking, BERT, and C-bit parity configurations at both the [edit interfaces ct3-fpc/pic/port<:channel> t3-options] and [edit interfaces t3-fpc/pic/port<:channel> t3-options] hierarchy levels, the Channelized T3-level statements are valid, and the T3-level statements are ignored.

If you include clocking, BERT, and C-bit parity configurations at both the [edit interfaces ct3-fpc/pic/port<:channel> t3-options] and [edit interfaces t1-fpc/pic/port<:channel> t1-options] hierarchy levels, the Channelized T3-level statements are operational for the T3 connections and the T1-level statements are operational for the T1 connections.

Because DS-0 channels do not have clocking capability, you must configure clocking at the [edit interfaces ct1-fpc/pic/port<:channel> t1-options] or [edit interfaces ce1-fpc/pic/port<:channel> e1-options] hierarchy level for Channelized NxDS-0 QPP interfaces.

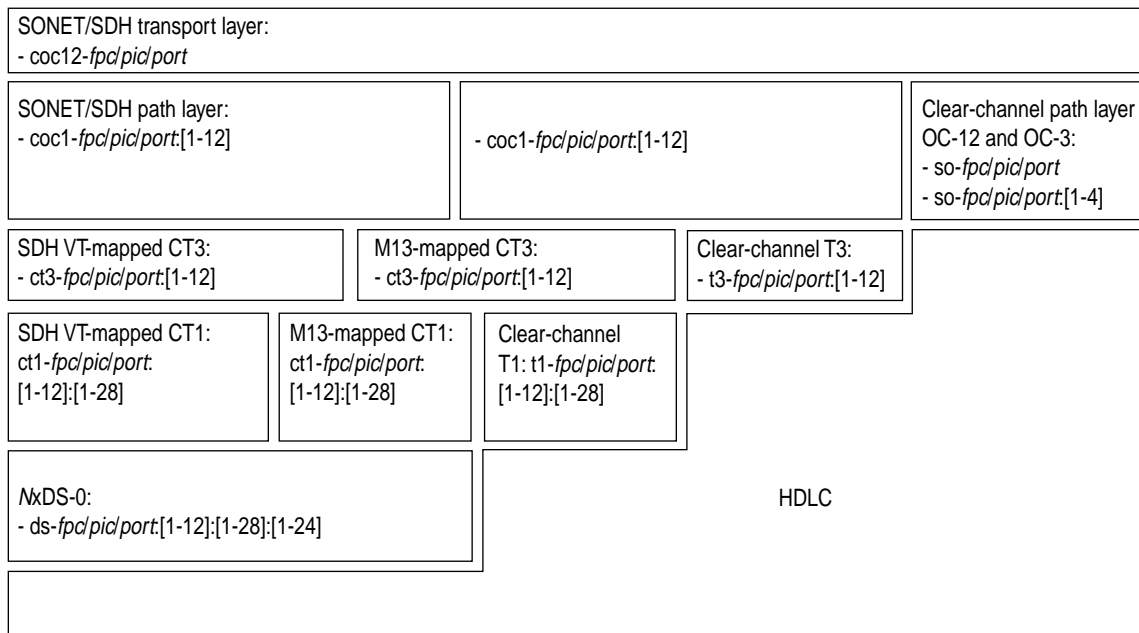
You can set BERT at the [edit interfaces t3-fpc/pic/port<:channel> t3-options] hierarchy level or on any partitioned channel of the Channelized T3 interface. There are twelve BERT patterns available for NxDS-0 channels and twenty-eight BERT patterns for T1, Channelized T1, T3, and Channelized T3 interfaces within channelized QPP interfaces.

For channelized interfaces that use Frame Relay encapsulation, the number of configurable data-link connection identifiers (DLCIs) varies by channelized interface type.

Structure of Channelized PICs with QPP

Figure 8, Figure 10, Figure 11, and Figure 11 show the structural organization of the Channelized OC-12 PIC with QPP, Channelized STM-1 PIC with QPP, Channelized DS-3 PIC with QPP, and Channelized E1 PIC with QPP. Table 17 on page 172 shows the structure of all channelized PICs, including channelized PICs with QPP and channelized PICs.

Figure 8: Structure of the Channelized OC-12 PIC with QPP



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Figure 9: Structure of the Channelized STM-1 PIC with QPP

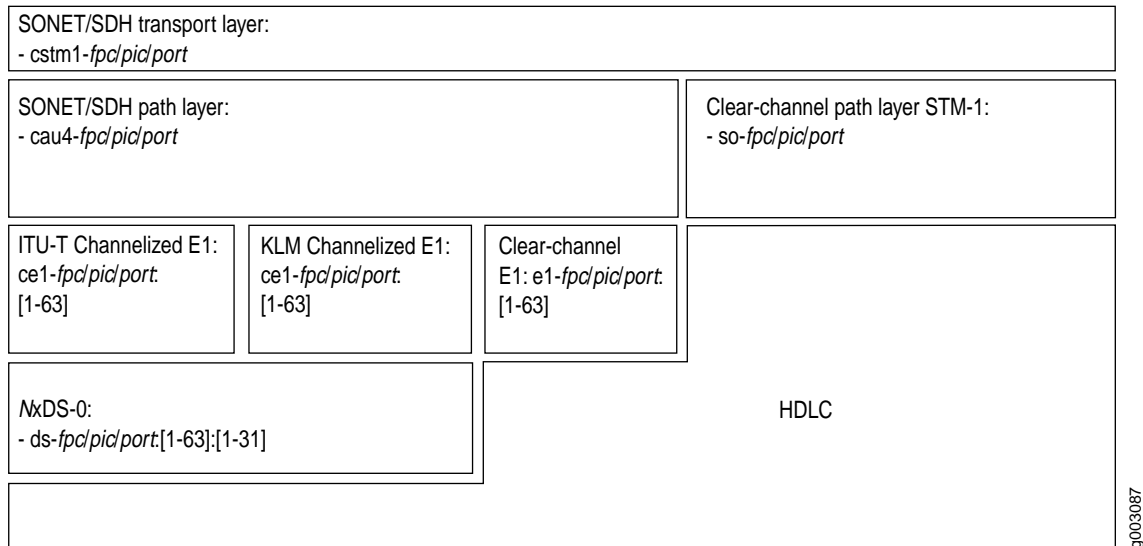


Figure 10: Structure of the Channelized DS-3 PIC with QPP

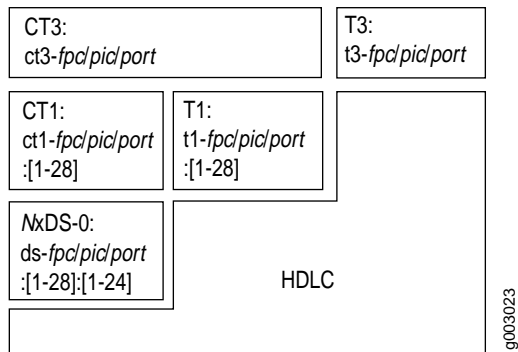


Figure 11: Structure of the Channelized E1 PIC with QPP

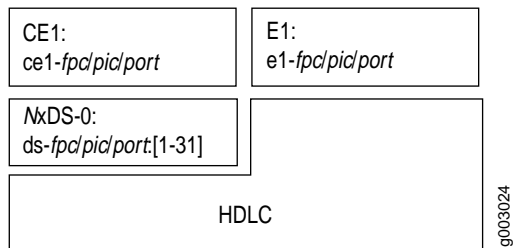


Table 17: Structural Differences: Channelized PICs and Channelized PICs with QPP

PIC Type	Transport	Path	DS-3	DS-1/E1
Channelized PICs				
Channelized OC-12	t3-fpc/pic/port:0	t3-fpc/pic/port:[0-11]	t3-fpc/pic/port:[0-11]	Not applicable.
Channelized T3 and Multichannel T3	Not applicable.	Not applicable.	t1-fpc/pic/port:0	t1-fpc/pic/port:[0-27]
Channelized STM-1	e1-fpc/pic/port:0	e1-fpc/pic/port:0	Not applicable.	e1-fpc/pic/port:[0-63]
Channelized E1	Not applicable.	Not applicable.	Not applicable.	e1-fpc/pic/port ds-fpc/pic/port:0
Channelized PICs with QPP				
Channelized OC-12 with QPP	coc12-fpc/pic/port	coc1-fpc/pic/port:[1-12]]so-fpc/pic/port	ct3-fpc/pic/port:[1-12] t3-fpc/pic/port:[1-12]	ct1-fpc/pic/port:[1-12]:[1-28] t1-fpc/pic/port:[1-12]:[1-28]]
Channelized STM-1 with QPP	Not applicable.	cau4-fpc/pic/port so-fpc/pic/port	Not applicable.	ce1-fpc/pic/port:[1-63] e1-fpc/pic/port:[1-63]
Channelized DS-3 with QPP	Not applicable.	Not applicable.	ct3-fpc/pic/port t3-fpc/pic/port	ct1-fpc/pic/port:[1-28] t1-fpc/pic/port:[1-28]
Channelized E1 with QPP	Not applicable.	Not applicable.	Not applicable.	ce1-fpc/pic/port e1-fpc/pic/port