

T320 Component Redundancy

The T320 Core Router is designed so that no single point of failure can cause the entire system to fail. The following major hardware components are redundant:

- Switch Interface Boards (SIBs)—The router has three SIBs. Each Type 1 FPC and Type 2 FPC has a dedicated ASIC with five high-speed links that connect to the SIBs (one link per SIB). A Type 3 FPC has two dedicated ASICs, and each ASIC has five high-speed links that connect to the SIBs (a total of 10 links). One of the three SIBs—usually SIB0—acts as a backup to the remaining two SIBs. In the event of a SIB failure, the backup SIB becomes active and traffic forwarding continues without any degradation. When the failed SIB is replaced, it becomes the new backup.
- Host subsystem—The host subsystem consists of a Routing Engine functioning together with a T-CB. The router can have one or two host subsystems. If two host subsystems are installed, one functions as the master and the other functions as the backup. If the master host subsystem (or either of its components) fails, the backup can take over as the master. To operate, each host subsystem requires a Routing Engine installed in an adjacent slot to a T-CB.
- SONET Clock Generators (SCGs)—The router has a standard configuration of one SCG, but a second can be purchased to function as backup. If one SCG fails, the other becomes the master SCG. Mastership of the SCGs is independent of the host subsystem, so routing functions are not affected.
- Power supplies—The router has two power supplies, which share the load evenly. If one power supply fails, the other power supply can provide full power to the routing node indefinitely.
- Cooling system—The cooling system has redundant components, which are controlled by the host subsystem. If one of the fans fails, the host subsystem increases the speed of the remaining fans to provide sufficient cooling for the router indefinitely.

- Related Topics**
- Reinstalling T320 Components in the Chassis
 - T320 Router Description
 - T320 System Architecture Description

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